



H57H-LM

Rev : 1.1

ECS CONFIDENTIAL

TABLE OF CONTENTS

Page	Index	Page	Index
1	COVER PAGE	24	PCI SLOT
2	Block Diagram	25	COM & PS2 & Fan
3	CPU MISC&Flexible Display Interface	26	LPT & SPI & LPC
4	CPU DMI&PEG&CFG	27	F_PANEL & Fan & ATX
5	CPU DDR3A/DDR3B	28	SUPER IO 8721
6	CPU Power	29	LAN Realtek 8111E
7	CPU GND&RSVD	30	Audio ALC662
8	PCI-E 16X / 1X	31	Audio Connector
9	CONN DDR3 CH A DIMM1	32	DC-DC CPU Vcore
10	CONN DDR3 CH A DIMM0	33	DC-DC V_AXG
11	CONN DDR3 CH B DIMM1	34	DC-DC PCH Core,VDIMM,V_1P8_SFR
12	CONN DDR3 CH B DIMM0	35	DC-DC CPU_VTT,5VDUAL
13	PCH USB&PCIE&DMI	36	GPIO Table & Other
14	PCH SATA,HOST,CLINK,PCI	37	Power Delivery
15	PCH GPIO,AUDIO,LPC,SPI	38	PWRGD&RST Tree
16	PCH Power,Decoupling	39	Clock Map
17	PCH GND / FDLINK/ NVRAM	40	History
18	PCH Video and DDSP		
19	PCH CLOCKS,Straps / TPM		
20	CLK GEN ICS9LRS4180		
21	Primary&PCH XDP		
22	VGA Connector / DVI connector		
23	USB Header & Port		


REVISION HISTORY:

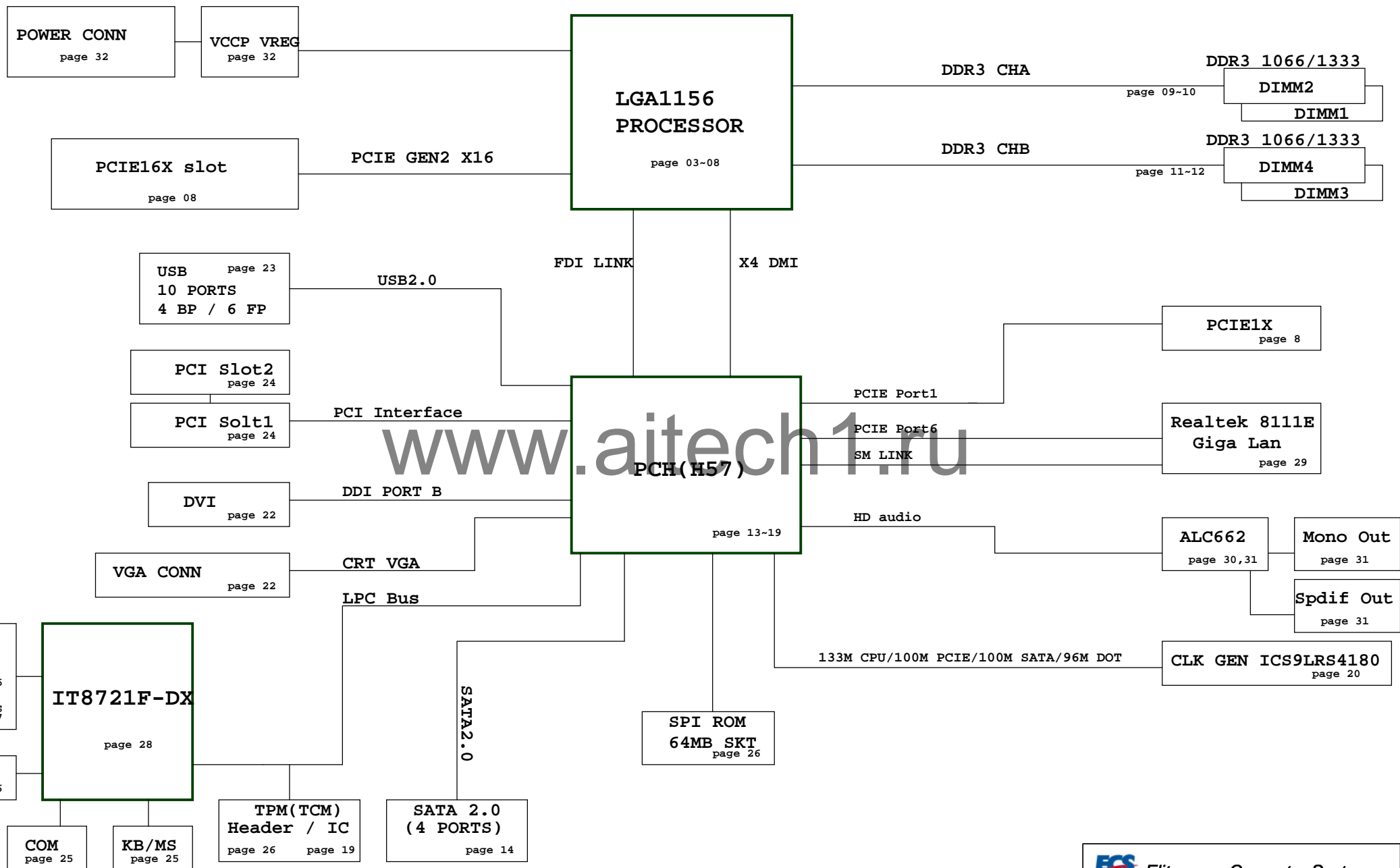
Rev	Date	Notes
V.A	2010/01/05	Initial version A3/ET stage
V1.0	2010/02/11	
V1.0A	2010/03/12	
V1.1	2010/04/02	For EuP lot6.0 2013(MB<0.1W) from H55 Change to H57

Note:

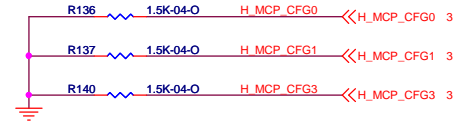
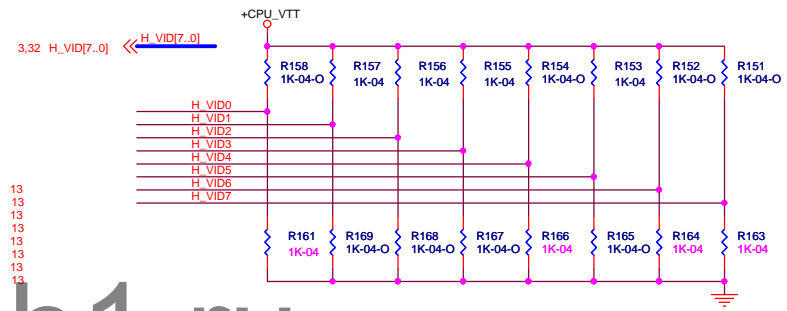
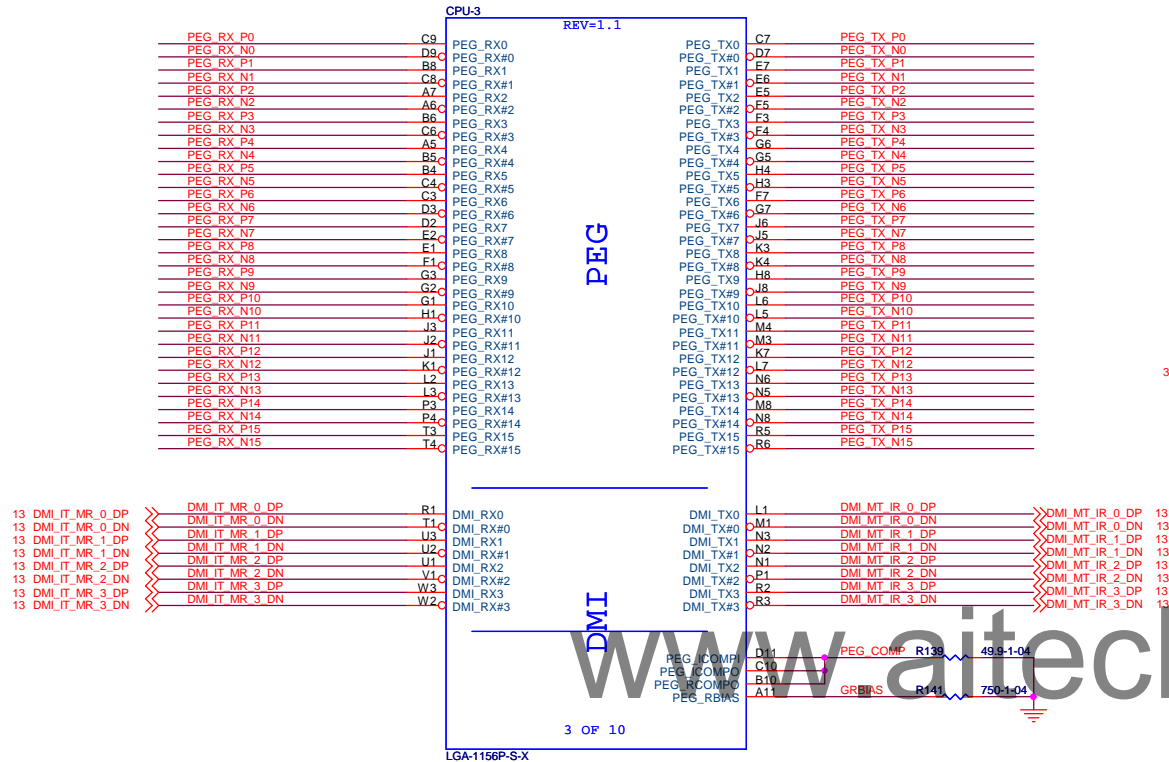
Design guide:

376563_376563_Piketon_Kings_Creek_Foxhollow_Platform_Design_Guide_Rev1_5

 Elitegroup Computer Systems			
Title Cover Page			
Size Custom	Document Number H57H-LM		Rev 1.1
Date: Friday, April 02, 2010	Sheet 1	of 40	



8 PEG_RX_P[0..15] >>>
8 PEG_RX_N[0..15] >>>
8 PEG_TX_P[0..15] <<<
8 PEG_TX_N[0..15] <<<



CFG	Desktop Lynnfield						
0	1	11=1*16X	0	10=2*8X	1	0	Reserved
1	1		1		0	0	
	Clarkdale PCI Express Static Lane Numbering Reversal				Lynnfield		
3	0	Reversal			Reserved		
	1	No Reversal					
	0,1,3 HAVE INTERNAL PULL-UPS						

POWER ON CONFIGURATION (POC)TABLE

	FUNCTION	Setting	Havendale	Lynnfield
VID0	MIS0	0	Support	Support
VID1	MIS1	1		
VID2	MIS2	1		
VID3	IMON CONFIG0	1	Icc(MAX)=110A	Icc(MAX)=110A
VID4	IMON CONFIG1	0		
VID5	IMON CONFIG2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		

Title
CPU DMI&PEG&CFG

Size
Custom

Date: Friday, April 02, 2010

Document Number
H57H-LM

Rev
1.1

Sheet 4 of 40

CPU-1

REV=1.1

M MA A A0	AW18	SA_MA[0]	SA_DQ00	AK3	M DOS A DP0
M MA A A1	AW15	SA_MA[1]	SA_DQ01	AK3	M DOS A DN0
M MA A A2	AW15	SA_MA[2]	SA_DQ00	AK2	M DQM A0
M MA A A3	AW15	SA_MA[3]	SA_DQ00	AK1	M DATA A0
M MA A A4	AW14	SA_MA[4]	SA_DQ01	AK2	M DATA A1
M MA A A5	AW13	SA_MA[5]	SA_DQ02	AK1	M DATA A2
M MA A A6	AW14	SA_MA[6]	SA_DQ03	AK2	M DATA A3
M MA A A7	AW14	SA_MA[7]	SA_DQ04	AK2	M DATA A4
M MA A A8	AW12	SA_MA[8]	SA_DQ05	AK1	M DATA A5
M MA A A9	AW12	SA_MA[9]	SA_DQ06	AK2	M DATA A6
M MA A A10	AT19	SA_MA[10]	SA_DQ07	AK2	M DATA A7
M MA A A11	AW13	SA_MA[11]	SA_DQ08	AK2	M DATA A8
M MA A A12	AW11	SA_MA[12]	SA_DQ09	AK2	M DATA A9
M MA A A13	AW11	SA_MA[13]	SA_DQ10	AK2	M DATA A10
M MA A A14	AT11	SA_MA[14]	SA_DQ11	AK2	M DATA A11
M MA A A15	AR10	SA_MA[15]	SA_DQ12	AK2	M DATA A12
M WE A L	AT22	SA_WE#	SA_DQ13	AK2	M DATA A13
M CAS A L	AW22	SA_CAS#	SA_DQ14	AK2	M DATA A14
M RAS A L	AT22	SA_RAS#	SA_DQ15	AK2	M DATA A15
M SBS A0	AV20	SA_BS[0]	SA_DQ16	AK2	M DATA A16
M SBS A1	AW19	SA_BS[1]	SA_DQ17	AK2	M DATA A17
M SBS A2	AW12	SA_BS[2]	SA_DQ18	AK2	M DATA A18
M SCS A N0	AV21	SA_CS[0]	SA_DQ19	AK2	M DATA A19
M SCS A N1	AW24	SA_CS[1]	SA_DQ20	AK2	M DATA A20
M SCS A N2	AW21	SA_CS[2]	SA_DQ21	AK2	M DATA A21
M SCS A N3	AW24	SA_CS[3]	SA_DQ22	AK2	M DATA A22
M SCKE A0	AW10	SA_CKE[0]	SA_DQ23	AK2	M DATA A23
M SCKE A1	AW10	SA_CKE[1]	SA_DQ24	AK2	M DATA A24
M SCKE A2	AW10	SA_CKE[2]	SA_DQ25	AK2	M DATA A25
M SCKE A3	AW10	SA_CKE[3]	SA_DQ26	AK2	M DATA A26
M ODT A0	AV23	SA_ODT[0]	SA_DQ27	AK2	M DATA A27
M ODT A1	AV24	SA_ODT[1]	SA_DQ28	AK2	M DATA A28
M ODT A2	AW23	SA_ODT[2]	SA_DQ29	AK2	M DATA A29
M ODT A3	AV24	SA_ODT[3]	SA_DQ30	AK2	M DATA A30
CK M DDR0 A DP	AR22	SA_CK[0]	SA_DQ31	AK2	M DATA A31
CK M DDR0 A DN	AR22	SA_CK[1]	SA_DQ32	AK2	M DATA A32
CK M DDR1 A DP	AP18	SA_CK[2]	SA_DQ33	AK2	M DATA A33
CK M DDR1 A DN	AN18	SA_CK[3]	SA_DQ34	AK2	M DATA A34
CK M DDR2 A DP	AP19	SA_CK[4]	SA_DQ35	AK2	M DATA A35
CK M DDR2 A DN	AN19	SA_CK[5]	SA_DQ36	AK2	M DATA A36
CK M DDR3 A DP	AP19	SA_CK[6]	SA_DQ37	AK2	M DATA A37
CK M DDR3 A DN	AN19	SA_CK[7]	SA_DQ38	AK2	M DATA A38
DDR3 DRAMRST_L	AV8	SM_DRAMRST#	SA_DQ39	AK2	M DATA A39
STP12	1 TP DDR0 CS4	AK22	SA_DQ40	AK2	M DATA A40
STP16	1 TP DDR0 CS5	AK22	SA_DQ41	AK2	M DATA A41
STP17	1 TP DDR0 CS6	AK23	SA_DQ42	AK2	M DATA A42
STP9	1 TP DDR0 CS7	AK23	SA_DQ43	AK2	M DATA A43
SA_DQ44	AK23	SA_DQ44	SA_DQ44	AK2	M DATA A44
SA_DQ45	AK23	SA_DQ45	SA_DQ45	AK2	M DATA A45
SA_DQ46	AK23	SA_DQ46	SA_DQ46	AK2	M DATA A46
SA_DQ47	AK23	SA_DQ47	SA_DQ47	AK2	M DATA A47
SA_DQ48	AK23	SA_DQ48	SA_DQ48	AK2	M DATA A48
SA_DQ49	AK23	SA_DQ49	SA_DQ49	AK2	M DATA A49
SA_DQ50	AK23	SA_DQ50	SA_DQ50	AK2	M DATA A50
SA_DQ51	AK23	SA_DQ51	SA_DQ51	AK2	M DATA A51
SA_DQ52	AK23	SA_DQ52	SA_DQ52	AK2	M DATA A52
SA_DQ53	AK23	SA_DQ53	SA_DQ53	AK2	M DATA A53
SA_DQ54	AK23	SA_DQ54	SA_DQ54	AK2	M DATA A54
SA_DQ55	AK23	SA_DQ55	SA_DQ55	AK2	M DATA A55
SA_DQ56	AK23	SA_DQ56	SA_DQ56	AK2	M DATA A56
SA_DQ57	AK23	SA_DQ57	SA_DQ57	AK2	M DATA A57
SA_DQ58	AK23	SA_DQ58	SA_DQ58	AK2	M DATA A58
SA_DQ59	AK23	SA_DQ59	SA_DQ59	AK2	M DATA A59
SA_DQ60	AK23	SA_DQ60	SA_DQ60	AK2	M DATA A60
SA_DQ61	AK23	SA_DQ61	SA_DQ61	AK2	M DATA A61
SA_DQ62	AK23	SA_DQ62	SA_DQ62	AK2	M DATA A62
SA_DQ63	AK23	SA_DQ63	SA_DQ63	AK2	M DATA A63

DDR_A

1 OF 10

LGA-1156P-S-X

CPU-2


REV=1.1

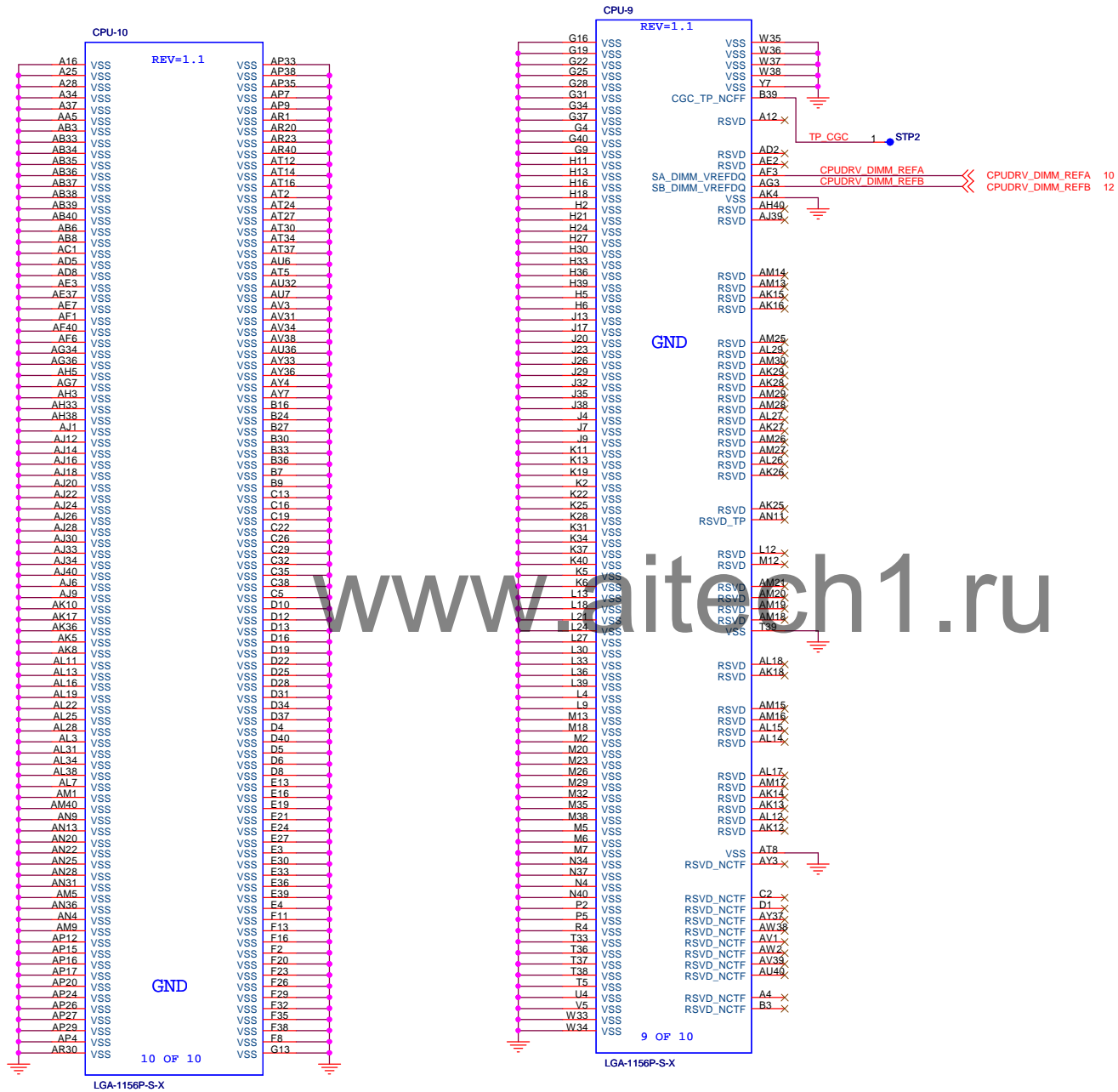
M MA A B0	AU20	SB_MA[0]	SB_DQ0[0]	AF4	M DOS B DP0
M MA A B1	AU18	SB_MA[1]	SB_DQ0[1]	AE5	M DOS B DN0
M MA A B2	AU18	SB_MA[2]	SB_DQ0[2]	AE4	M DQM B0
M MA A B3	AU17	SB_MA[3]	SB_DQ0[3]	AD7	M DATA B0
M MA A B4	AY18	SB_MA[4]	SB_DQ0[4]	AD8	M DATA B1
M MA A B5	AY17	SB_MA[5]	SB_DQ0[5]	AD8	M DATA B2
M MA A B6	AW17	SB_MA[6]	SB_DQ0[6]	AC7	M DATA B3
M MA A B7	AU16	SB_MA[7]	SB_DQ0[7]	AC5	M DATA B4
M MA A B8	AY17	SB_MA[8]	SB_DQ0[8]	AF5	M DATA B5
M MA A B9	AY16	SB_MA[9]	SB_DQ0[9]	AF5	M DATA B6
M MA A B10	AY25	SB_MA[10]	SB_DQ0[10]	AE6	M DATA B7
M MA A B11	AW16	SB_MA[11]	SB_DQ0[11]	AH6	M DOS B DP1
M MA A B12	AW15	SB_MA[12]	SB_DQ0[12]	AJ5	M DOS B DN1
M MA A B13	AW28	SB_MA[13]	SB_DQ0[13]	AH4	M DQM B1
M MA A B14	AY12	SB_MA[14]	SB_DQ0[14]	AG5	M DATA B8
M MA A B15	AY11	SB_MA[15]	SB_DQ0[15]	AH7	M DATA B9
M WE B L	AU26	SB_WE#	SB_DQ0[16]	AK6	M DATA B10
M CAS B L	AW27	SB_CAS#	SB_DQ0[17]	AG6	M DATA B11
M RAS B L	AW26	SB_RAS#	SB_DQ0[18]	AG4	M DATA B12
M SBS B0	AU25	SB_BS[0]	SB_DQ0[19]	AG4	M DATA B13
M SBS B1	AW25	SB_BS[1]	SB_DQ0[20]	AJ7	M DATA B14
M SBS B2	AY12	SB_BS[2]	SB_DQ0[21]	AK7	M DATA B15
M SCS B N0	AY27	SB_CS[0]	SB_DQ0[22]	AN6	M DOS B DP2
M SCS B N1	AW29	SB_CS[1]	SB_DQ0[23]	AM6	M DOS B DN2
M SCS B N2	AY26	SB_CS[2]	SB_DQ0[24]	AM7	M DQM B2
M SCS B N3	AY29	SB_CS[3]	SB_DQ0[25]	AL6	M DATA B16
M SCKE B0	AW8	SB_CKE[0]	SB_DQ0[26]	AN6	M DATA B17
M SCKE B1	AW8	SB_CKE[1]	SB_DQ0[27]	AP6	M DATA B18
M SCKE B2	AW8	SB_CKE[2]	SB_DQ0[28]	AR5	M DATA B19
M SCKE B3	AW8	SB_CKE[3]	SB_DQ0[29]	AL5	M DATA B20
M ODT B0	AU27	SB_ODT[0]	SB_DQ0[30]	AM4	M DATA B21
M ODT B1	AU27	SB_ODT[1]	SB_DQ0[31]	AN7	M DATA B22
M ODT B2	AU27	SB_ODT[2]	SB_DQ0[32]	AP5	M DATA B23
M ODT B3	AU28	SB_ODT[3]	SB_DQ0[33]	AR8	M DOS B DP3
CK M DDR0 B DP	AR17	SB_CK[0]	SB_DQ0[34]	AP8	M DOS B DN3
CK M DDR0 B DN	AR16	SB_CK[1]	SB_DQ0[35]	AT7	M DQM B3
CK M DDR1 B DP	AT15	SB_CK[2]	SB_DQ0[36]	AT6	M DATA B24
CK M DDR1 B DN	AR15	SB_CK[3]	SB_DQ0[37]	AR7	M DATA B25
CK M DDR2 B DP	AN17	SB_CK[4]	SB_DQ0[38]	AR9	M DATA B26
CK M DDR2 B DN	AN16	SB_CK[5]	SB_DQ0[39]	AM8	M DATA B27
CK M DDR3 B DP	AR19	SB_CK[6]	SB_DQ0[40]	AN8	M DATA B28
CK M DDR3 B DN	AR18	SB_CK[7]	SB_DQ0[41]	AR6	M DATA B29
STP15	1 TP DDR1 CS4	AK23	SB_DQ0[42]	AL8	M DATA B30
STP11	1 TP DDR1 CS5	AK23	SB_DQ0[43]	AT9	M DATA B31
STP18	1 TP DDR1 CS6	AK24	SB_DQ0[44]	AT25	M DOS B DP4
STP13	1 TP DDR1 CS7	AK24	SB_DQ0[45]	AR24	M DOS B DN4
SA_DQ46	AK24	SA_DQ46	SA_DQ46	AN4	M DQM B4
SA_DQ47	AK24	SA_DQ47	SA_DQ47	AN23	M DATA B32
SA_DQ48	AK24	SA_DQ48	SA_DQ48	AP23	M DATA B33
SA_DQ49	AK24	SA_DQ49	SA_DQ49	AR25	M DATA B34
SA_DQ50	AK24	SA_DQ50	SA_DQ50	AR26	M DATA B35
SA_DQ51	AK24	SA_DQ51	SA_DQ51	AT23	M DATA B36
SA_DQ52	AK24	SA_DQ52	SA_DQ52	AP22	M DATA B37
SA_DQ53	AK24	SA_DQ53	SA_DQ53	AP25	M DATA B38
SA_DQ54	AK24	SA_DQ54	SA_DQ54	AT26	M DATA B39
SA_DQ55	AK24	SA_DQ55	SA_DQ55	AP32	M DOS B DP5
SA_DQ56	AK24	SA_DQ56	SA_DQ56	AR32	M DOS B DN5
SA_DQ57	AK24	SA_DQ57	SA_DQ57	AN32	M DQM B5
SA_DQ58	AK24	SA_DQ58	SA_DQ58	AT32	M DATA B40
SA_DQ59	AK24	SA_DQ59	SA_DQ59	AP31	M DATA B41
SA_DQ60	AK24	SA_DQ60	SA_DQ60	AR33	M DATA B42
SA_DQ61	AK24	SA_DQ61	SA_DQ61	AM32	M DATA B43
SA_DQ62	AK24	SA_DQ62	SA_DQ62	AT31	M DATA B44
SA_DQ63	AK24	SA_DQ63	SA_DQ63	AR31	M DATA B45
SA_DQ64	AK24	SA_DQ64	SA_DQ64	AR34	M DATA B46
SA_DQ65	AK24	SA_DQ65	SA_DQ65	AT33	M DATA B47
SA_DQ66	AK24	SA_DQ66	SA_DQ66	AR36	M DOS B DP6
SA_DQ67	AK24	SA_DQ67	SA_DQ67	AR37	M DOS B DN6
SA_DQ68	AK24	SA_DQ68	SA_DQ68	AM33	M DQM B6
SA_DQ69	AK24	SA_DQ69	SA_DQ69	AR35	M DATA B48
SA_DQ70	AK24	SA_DQ70	SA_DQ70	AT36	M DATA B49
SA_DQ71	AK24	SA_DQ71	SA_DQ71	AN33	M DATA B50
SA_DQ72	AK24	SA_DQ72	SA_DQ72	AP36	M DATA B51
SA_DQ73	AK24	SA_DQ73	SA_DQ73	AP34	M DATA B52
SA_DQ74	AK24	SA_DQ74	SA_DQ74	AT34	M DATA B53
SA_DQ75	AK24	SA_DQ75	SA_DQ75	AN34	M DATA B54
SA_DQ76	AK24	SA_DQ76	SA_DQ76	AP37	M DATA B55
SA_DQ77	AK24	SA_DQ77	SA_DQ77	AL37	M DOS B DP7
SA_DQ78	AK24	SA_DQ78	SA_DQ78	AM36	M DOS B DN7
SA_DQ79	AK24	SA_DQ79	SA_DQ79	AK35	M DQM B7
SA_DQ80	AK24	SA_DQ80	SA_DQ80	AL35	M DATA B56
SA_DQ81	AK24	SA_DQ81	SA_DQ81	AM35	M DATA B57
SA_DQ82	AK24	SA_DQ82	SA_DQ82	AJ36	M DATA B58
SA_DQ83	AK24	SA_DQ83	SA_DQ83	AN35	M DATA B59
SA_DQ84	AK24	SA_DQ84	SA_DQ84	AM34	M DATA B60
SA_DQ85	AK24	SA_DQ85	SA_DQ85	AJ35	M DATA B61
SA_DQ86	AK24	SA_DQ86	SA_DQ86	AL36	M DATA B62
SA_DQ87	AK24	SA_DQ87	SA_DQ87	AL36	M DATA B63

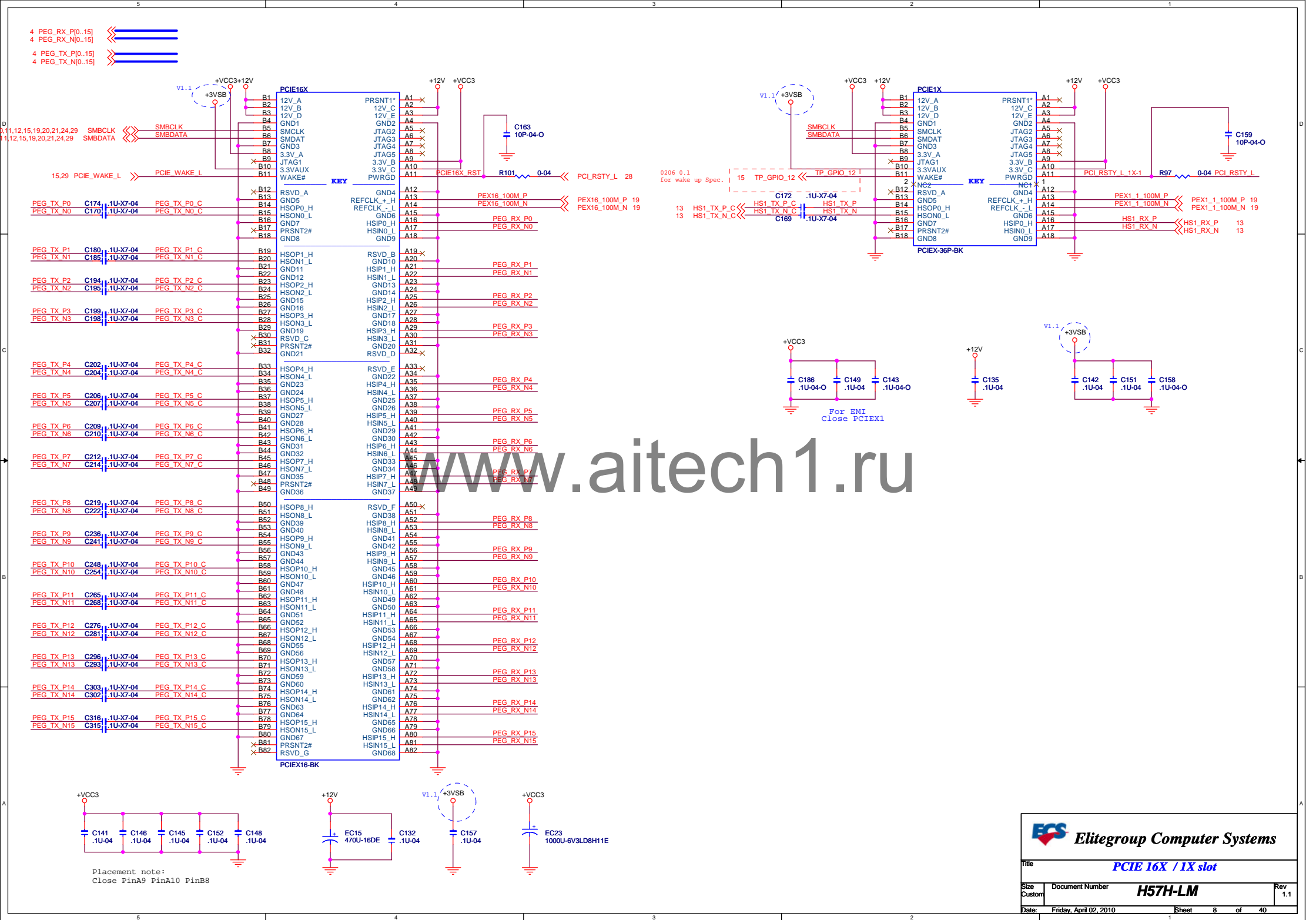
DDR_B

2 OF 10

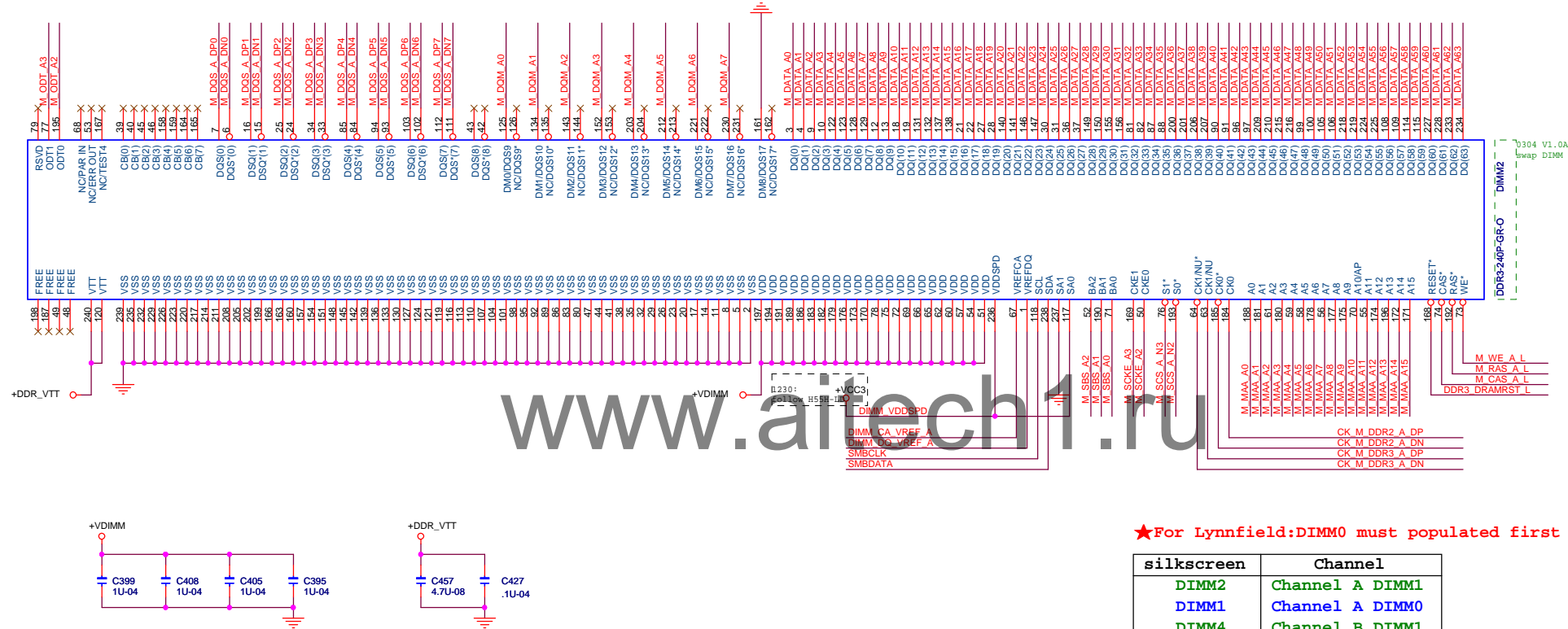
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 Elitegroup Computer Systems			
CPU DDR3A/DDR3B			
File	Document Number	Rev	
	H57H-LM	1.1	
Date:	Friday, April 02, 2010	Sheet	5 of 40





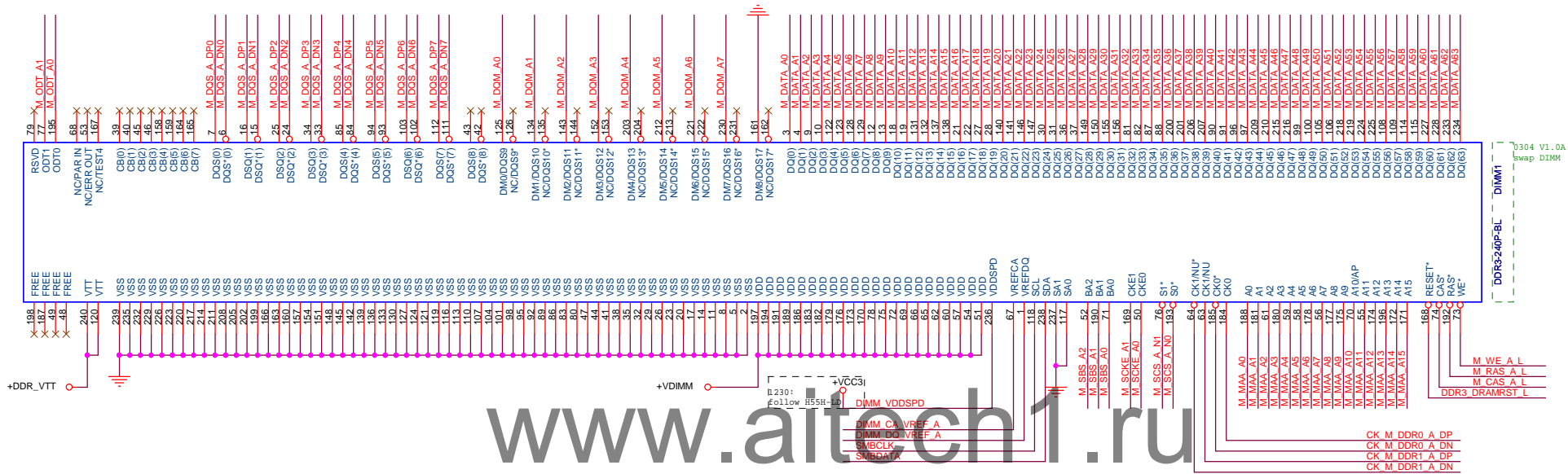
CHANNEL A DIMM1



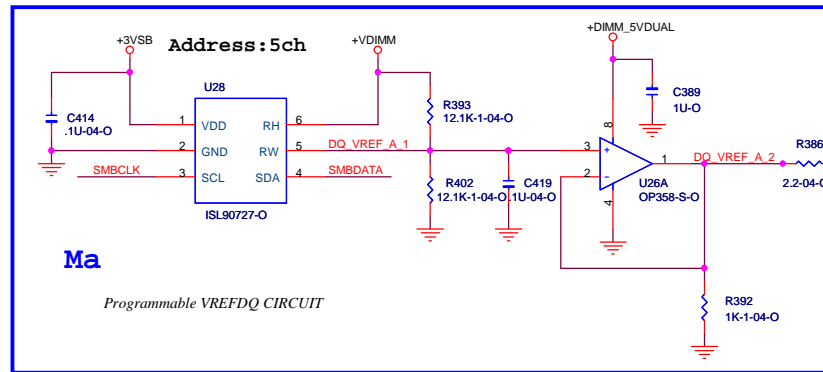
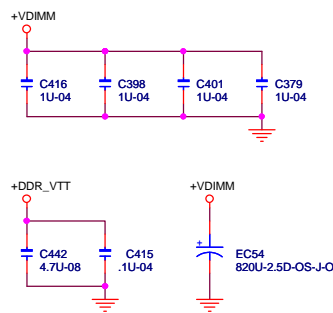
★For Lynnfield: DIMM0 must be populated first

silkscreen	Channel
DIMM2	Channel A DIMM1
DIMM1	Channel A DIMM0
DIMM4	Channel B DIMM1
DIMM3	Channel B DIMM0

CHANNEL A DIMM0

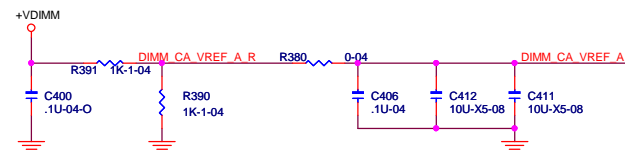


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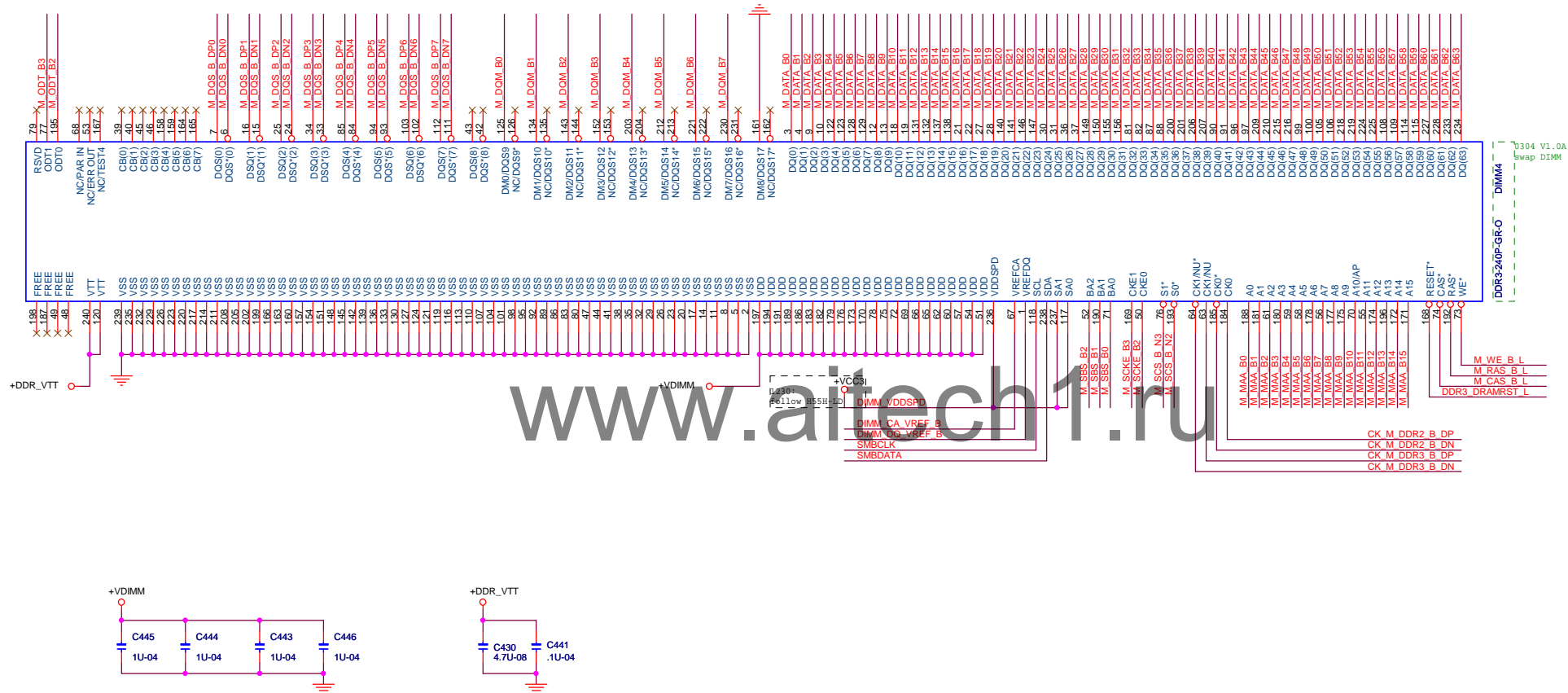


DQ_VREF Control Mode

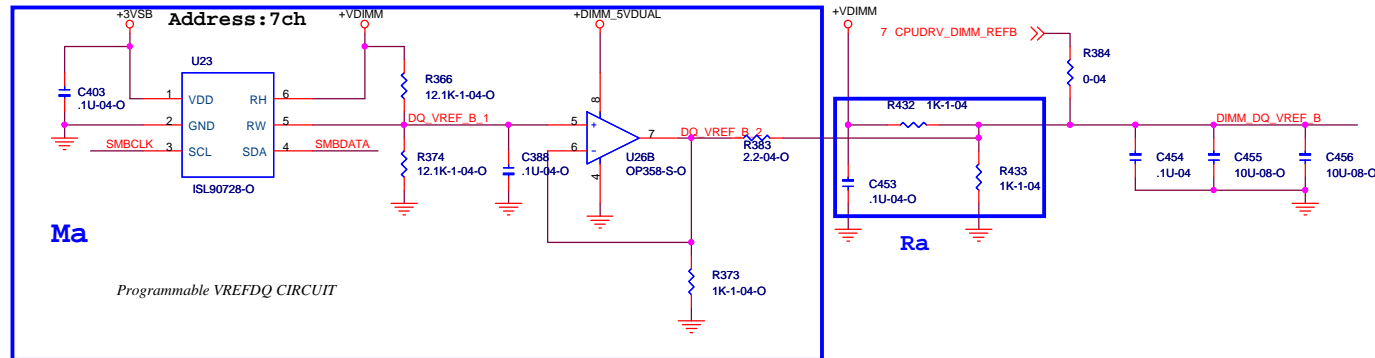
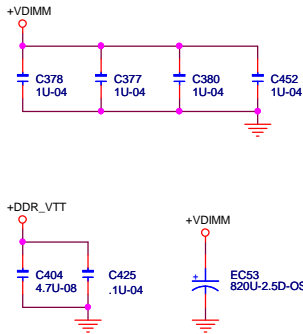
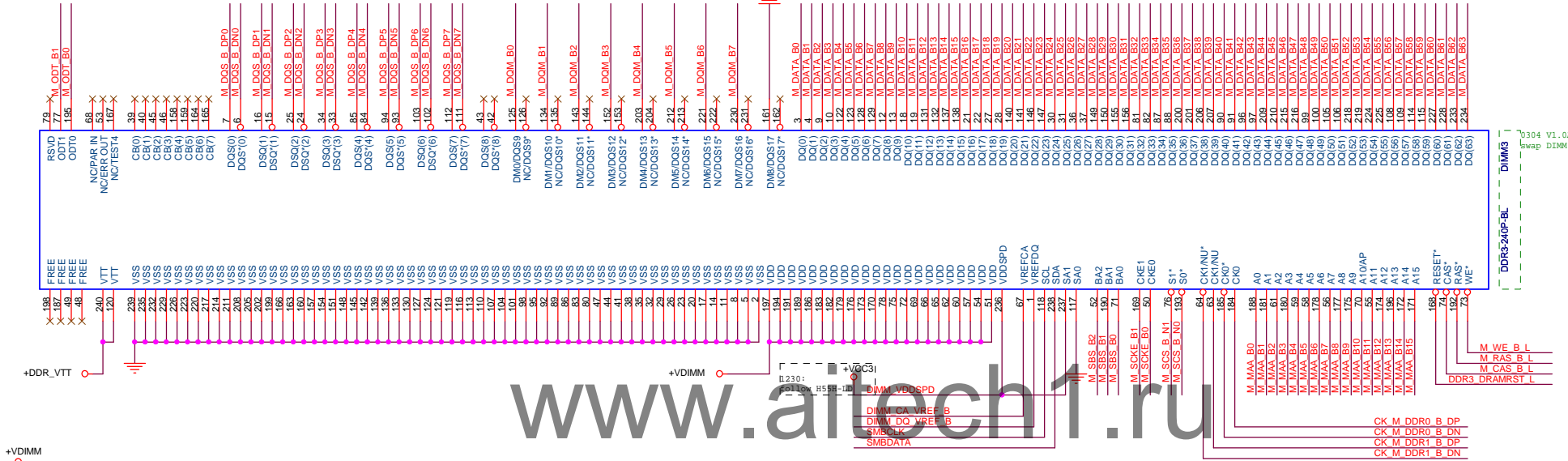
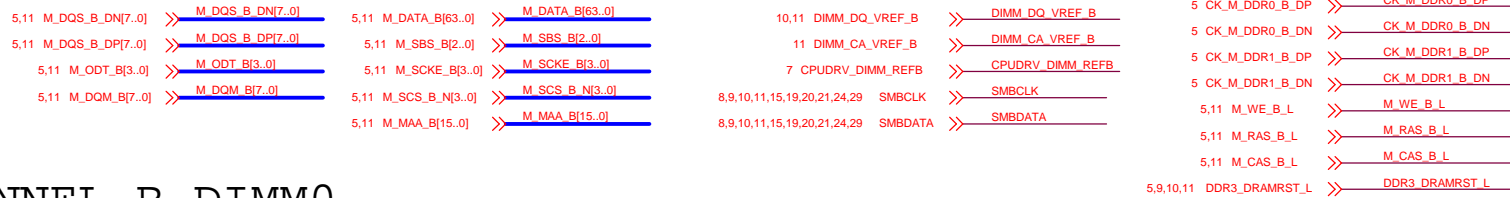
Mode 1	Ra
Mode 2	Ma

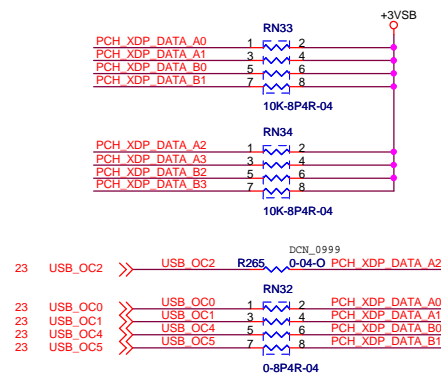
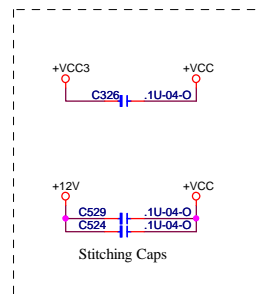
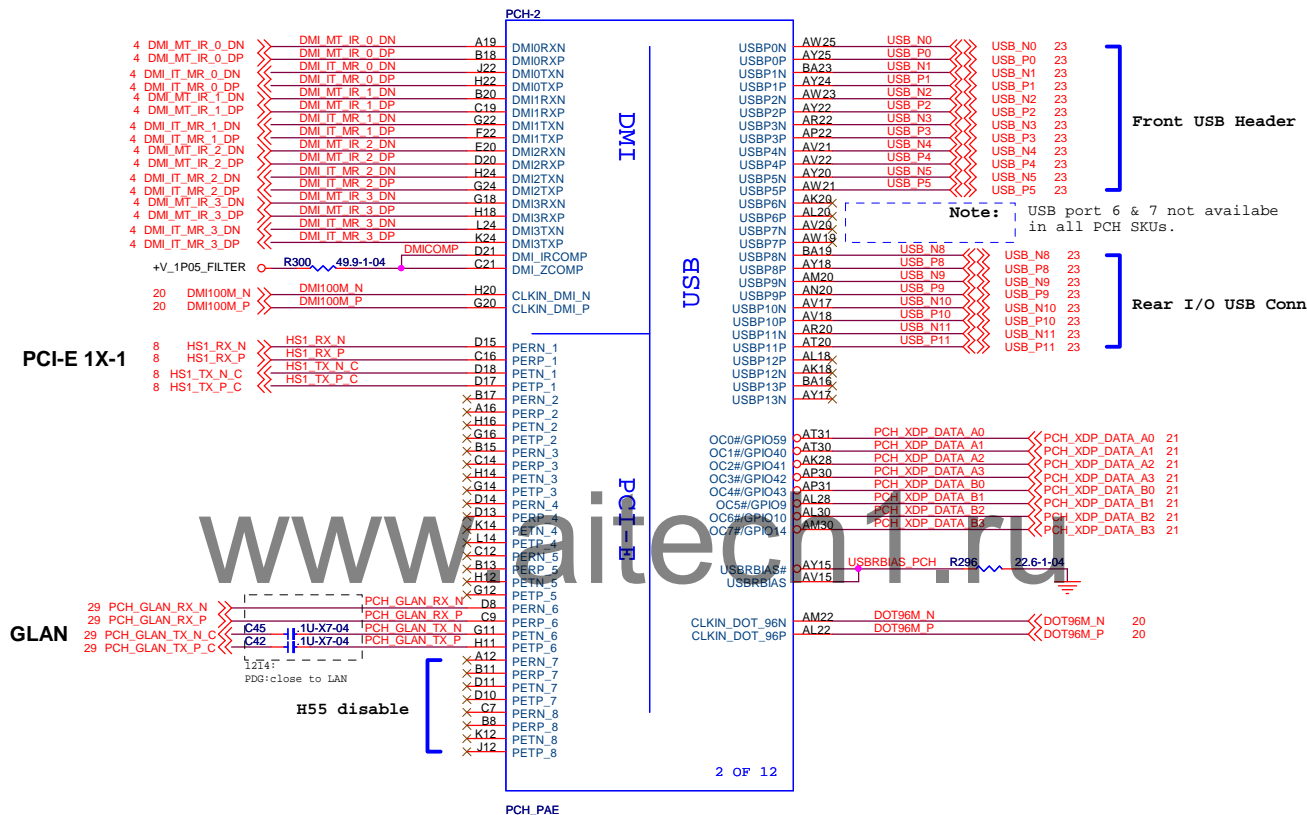


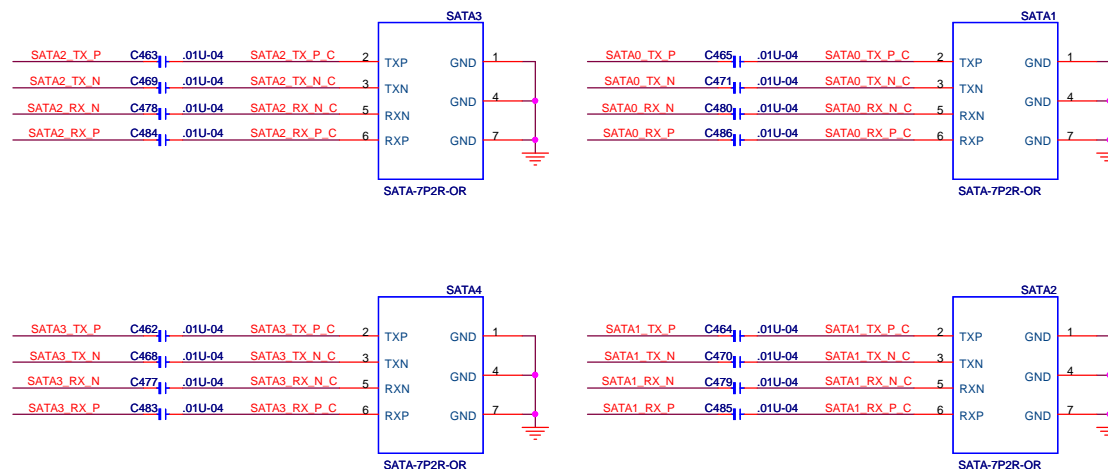
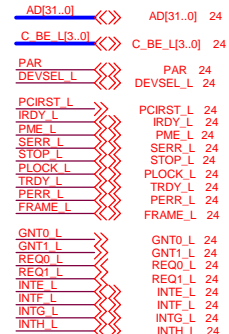
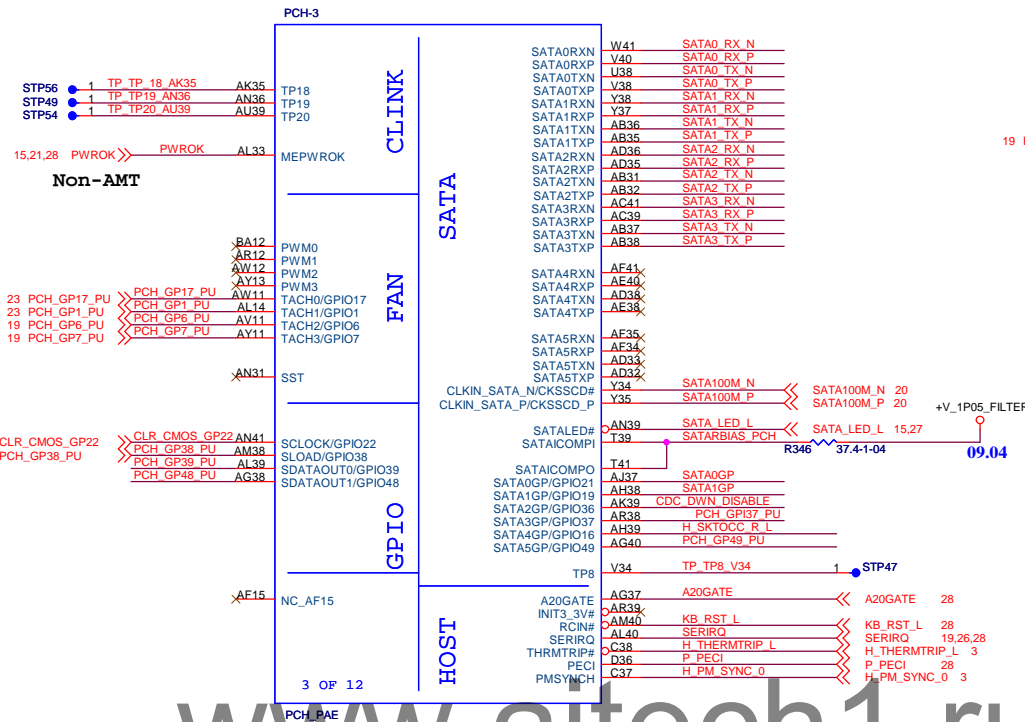
CHANNEL B DIMM1




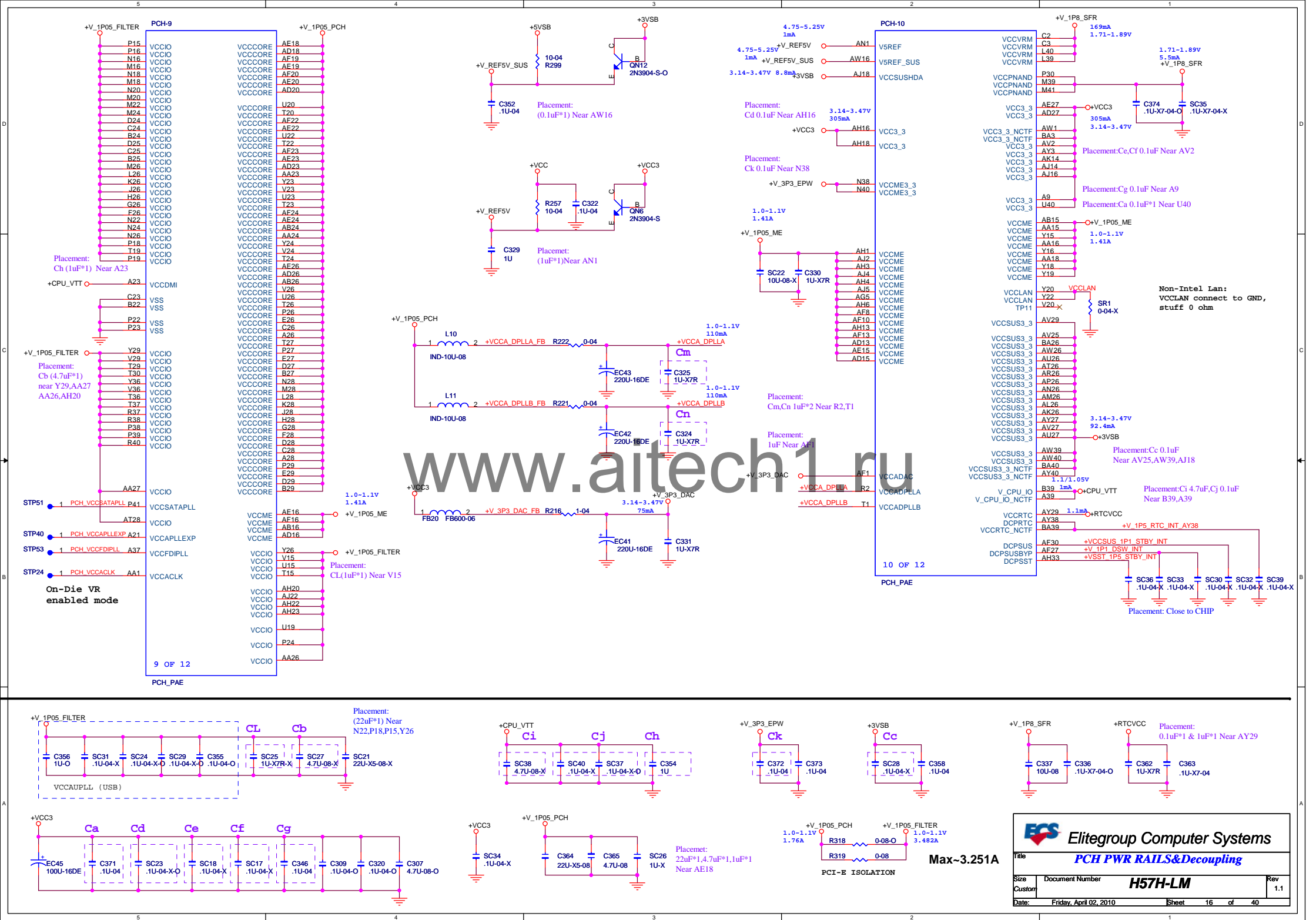
CHANNEL B DIMM0

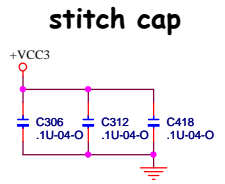
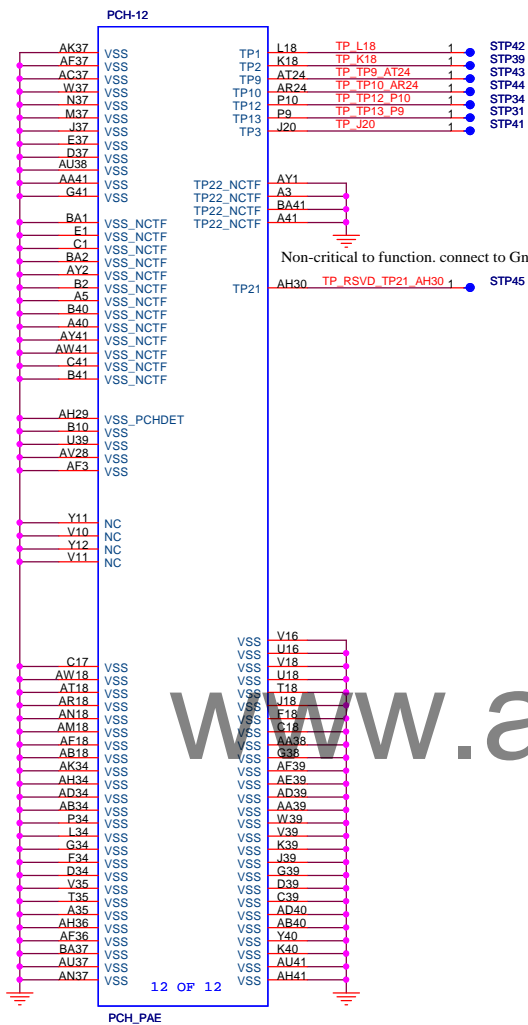
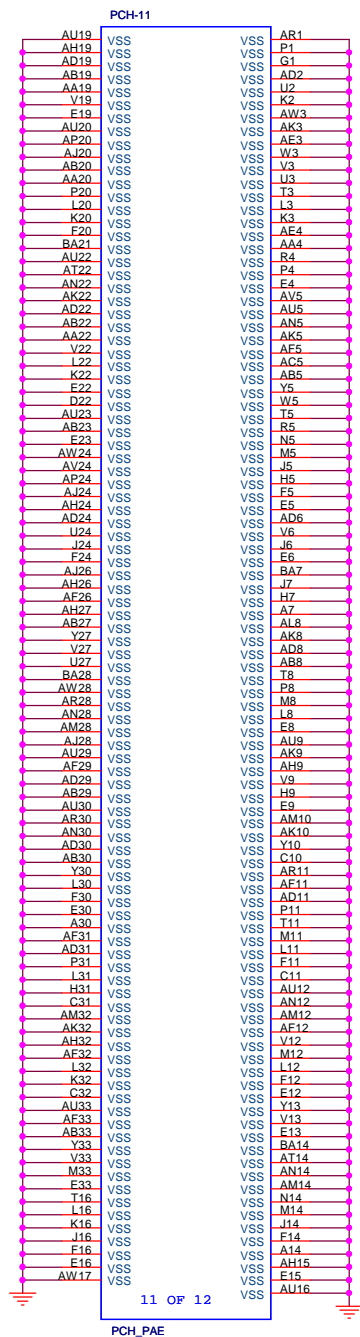




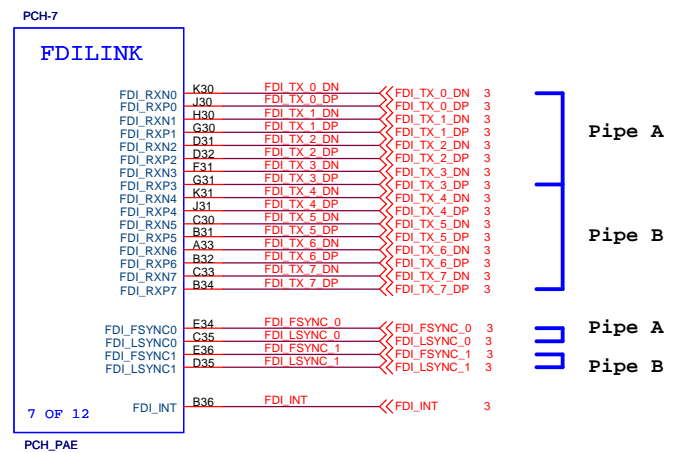


 Elitegroup Computer Systems				
File <i>PCB:SATA,HOST,CLINK,PCI</i>				
Size Custom	Document Number H57H-LM			Rev 1.1
Date: Friday, April 02, 2010		Sheet 14 of 40		

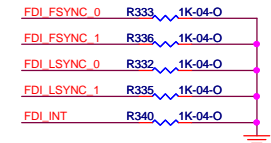




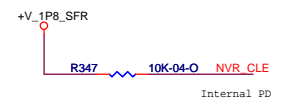
PCH FDI Link



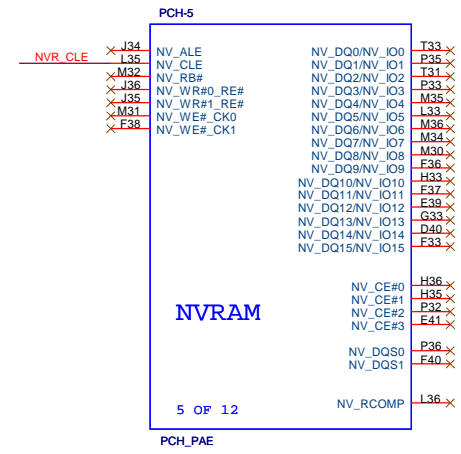
Stuff for Disable FDI



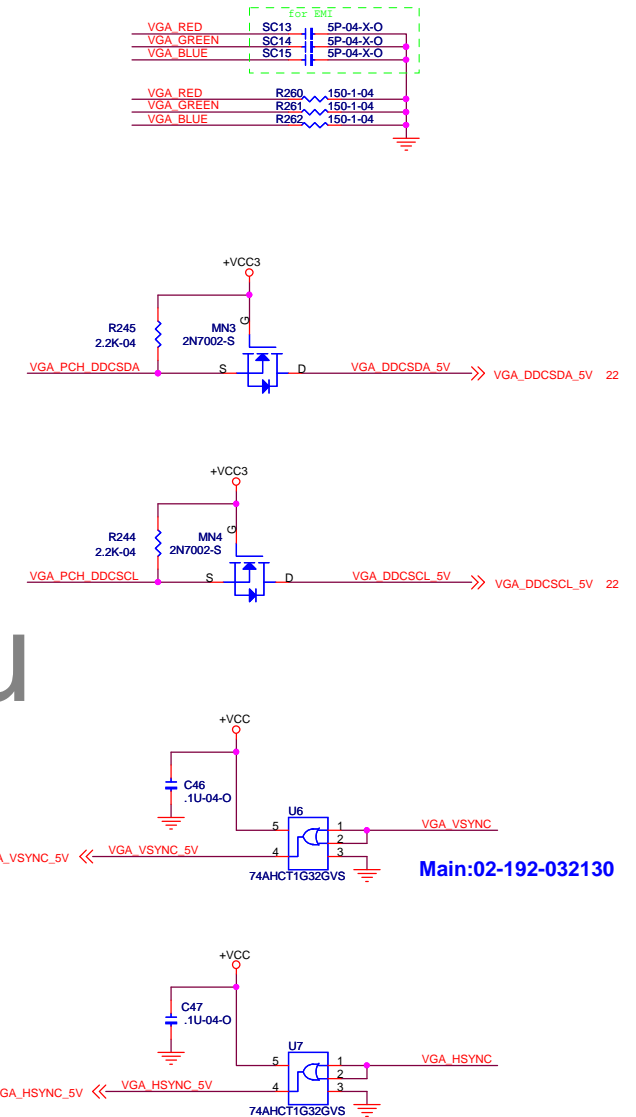
Note:
High:Enable Intel AT-d
Low:Disable Intel AT-d



NVRAM

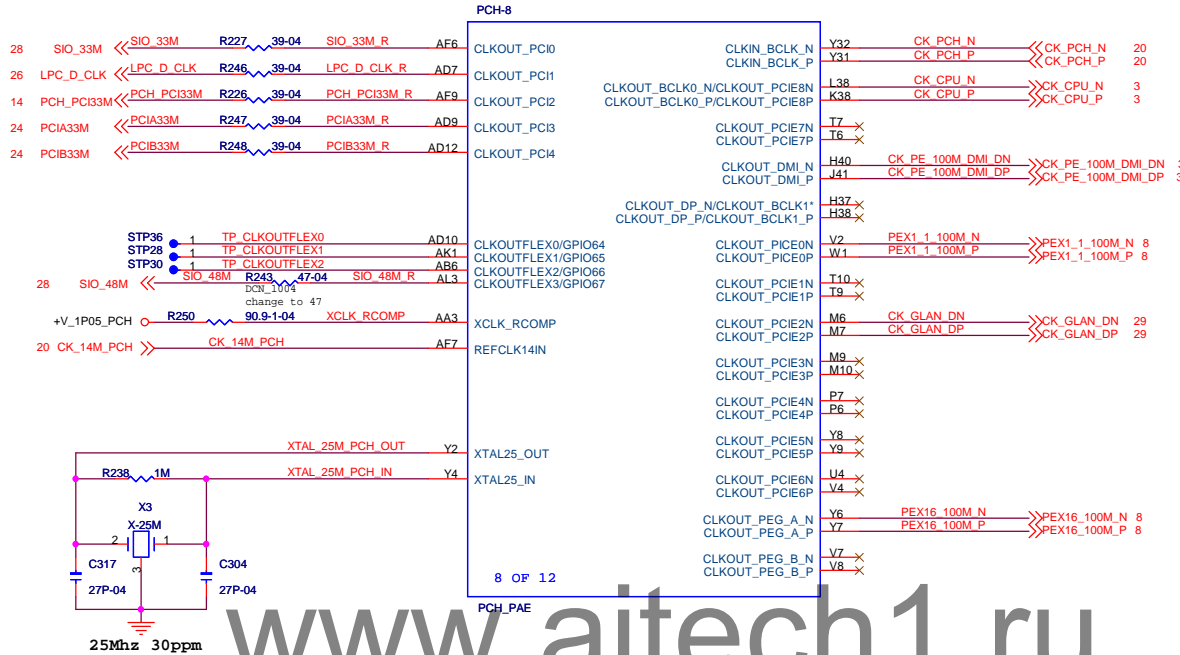
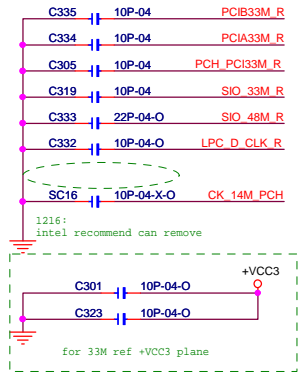


```
Port B:Capable of SDVO/HDMI/DVI/DP
Port C:Capable of HDMI/DVI/DP
Port D:Capable of HDMI/DVI/DP
```



Port	Strap	How to enable the port	How to Disable the Port
Port B	SDVO_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm	NC
Port C	DDPC_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm	NC
Port D	DDPD_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm	NC

SIO(33M)
TCM/TPMIC (33M)
PCI(PCH LB)
PCI slot1
PCI slot2



From CLK GEN

CPU(133M)

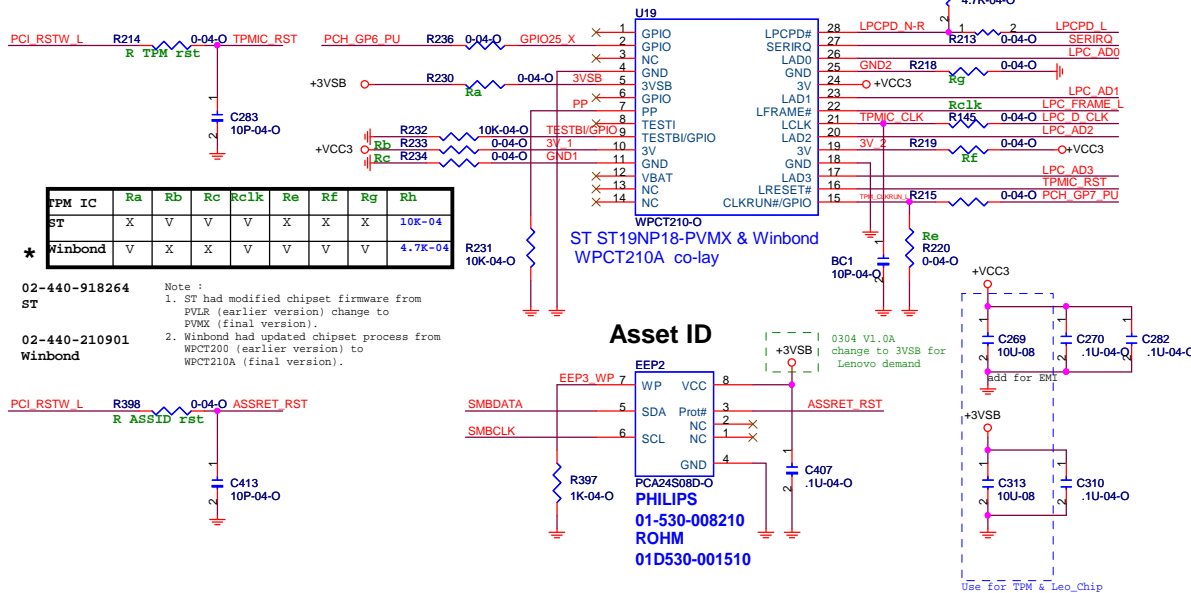
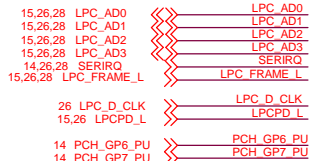
CPU(DMI)

PCIe-1 (1X)

Giga LAN

PCIe(16X)

TPM & Asset ID Function



CPU Strap Function

CFG	Havendale	Lynnfield			
0	REVERSED	1	11=1*16X	0	10=2*8X
1	REVERSED	1		1	
2	REVERSED				REVERSED
3	Static Lane Number Reversal				REVERSED
4	REVERSED				REVERSED
6	REVERSED				
7	REVERSED				
15	REVERSED				
0,1,2,3,4,5 ALL HAVE INTERNAL PULL-UPS					

POWER ON CONFIGURATION (POC) TABLE

	FUNCTION	Setting	Clarkdale	Lynnfield
VID0	MIS0	0	Support	Support
VID1	MIS1	1		
VID2	MIS2	1		
VID3	IMON CONFIG0	1	Icc(MAX)=110A	Icc(MAX)=110A
VID4	IMON CONFIG1	0		
VID5	IMON CONFIG2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		

Clock(ICS9LRS4180) Strap Function

Functionality Table FSLC,FSLA = 01, CPU_CLK = 133MHz

Bit2 FSLC	Bit1 FSLB	Bit0 FSLA	CPU MHZ	PCIEX MHZ	SATA MHZ	DOT96 MHZ
0	0	1	133.33	100.00	100.00	96.00
1	0	1	100.00	100.00	100.00	96.00

PCIEX PLL Spread Frequency Selection Table

B19b4	B19b3	FSLC B0b2	FSLB B0b1	FSLA B0b0	PCIEX MHZ	Spread %
0	0	0	0	1	100.00	0.5% Down
0	0	1	0	1	100.00	0.5% Down
1	0	0	0	1	100.00	NO Spread
1	0	1	0	1	100.00	NO Spread

CPU PLL Spread Frequency Selection Table

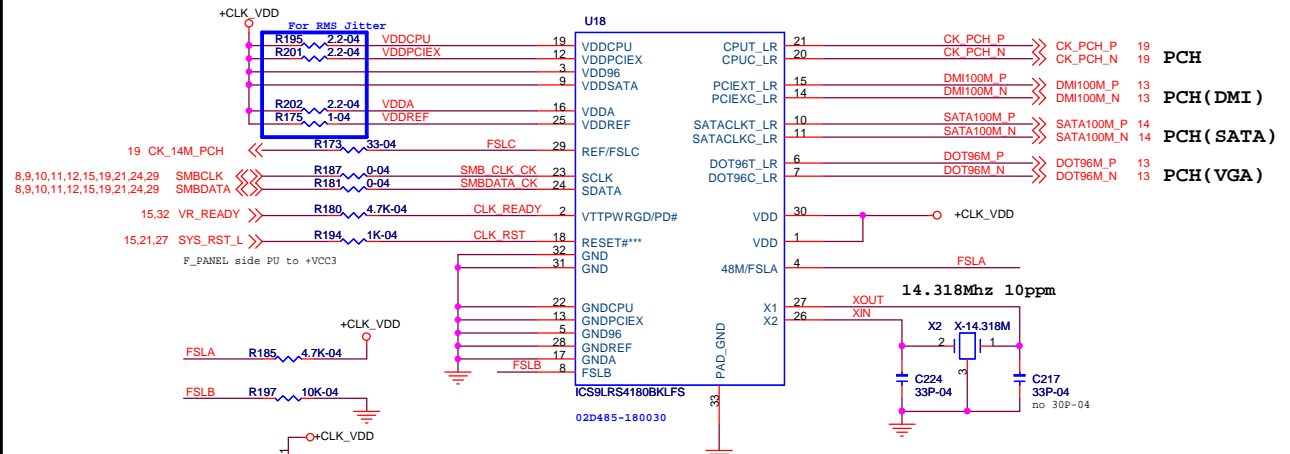
FSLC B0b2	FSLB B0b1	FSLA B0b0	CPU MHZ	Spread% B0b5=1
0	0	1	133.33	0.5% Down
1	0	1	100.00	0.5% Down

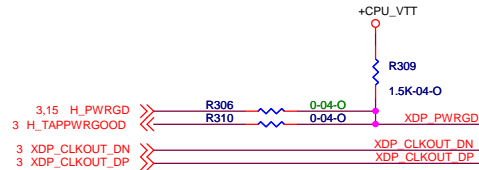
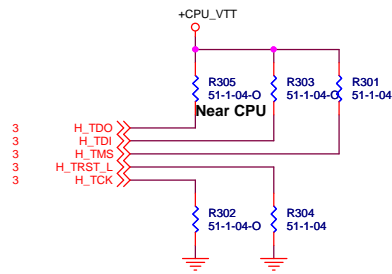
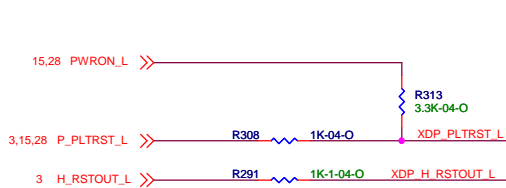
CPU CLK Table

Bit 0 FSLA	Bit 1 FSLB	Bit 2 FSLC	CPU CLK(MHz)	Default Setting
1	0	0	133	*
1	0	1	100	

PCH Strap Function

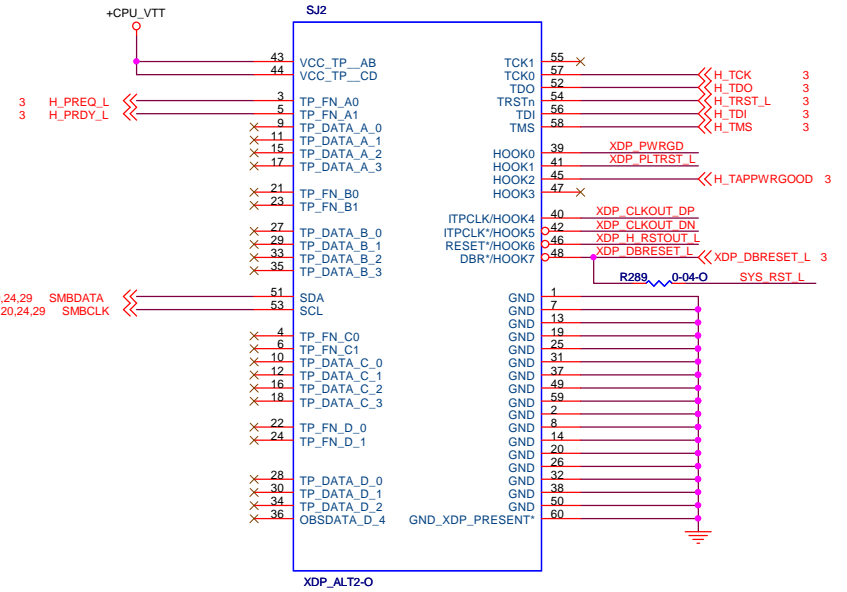
BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1



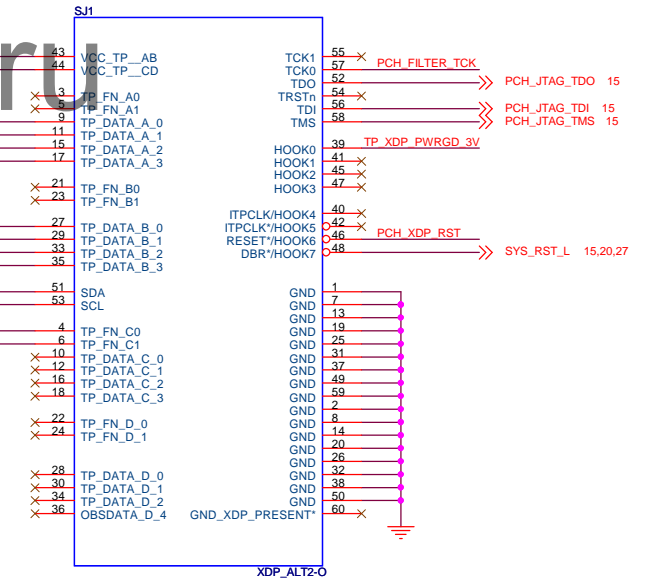
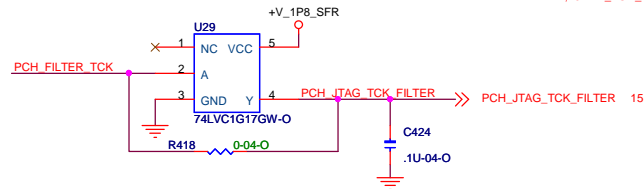
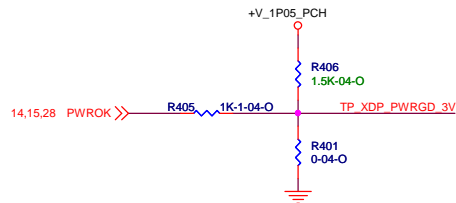
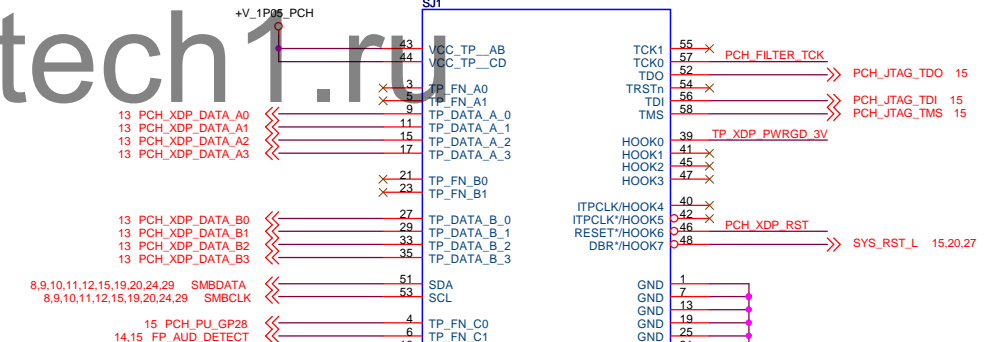
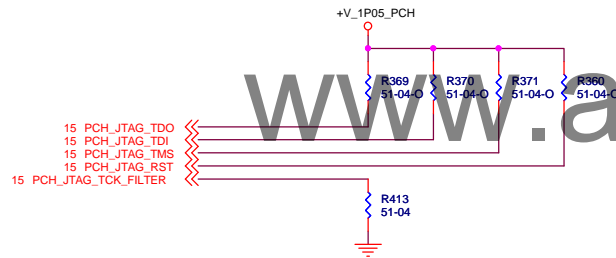


CLK Source:Default use PCH

8,9,10,11,12,15,19,20,24,29 SMBDATA
8,9,10,11,12,15,19,20,24,29 SMBCLK



DESIGN NOTE:
DEFAULT EMPTY SITE ON PAGE 94: XDP_PWROD RES (R108PR) TO VTT_OUT_RIGHT
DEFAULT EMPTY SITE ON PAGE 123: XDP_PWROD RES (R3S3EV) TO V_FSB_VTT
DEFAULT STUFF SITE: (R662EV) TO TP_XDP_PWROD



DESIGN NOTE:
PCH JTAG

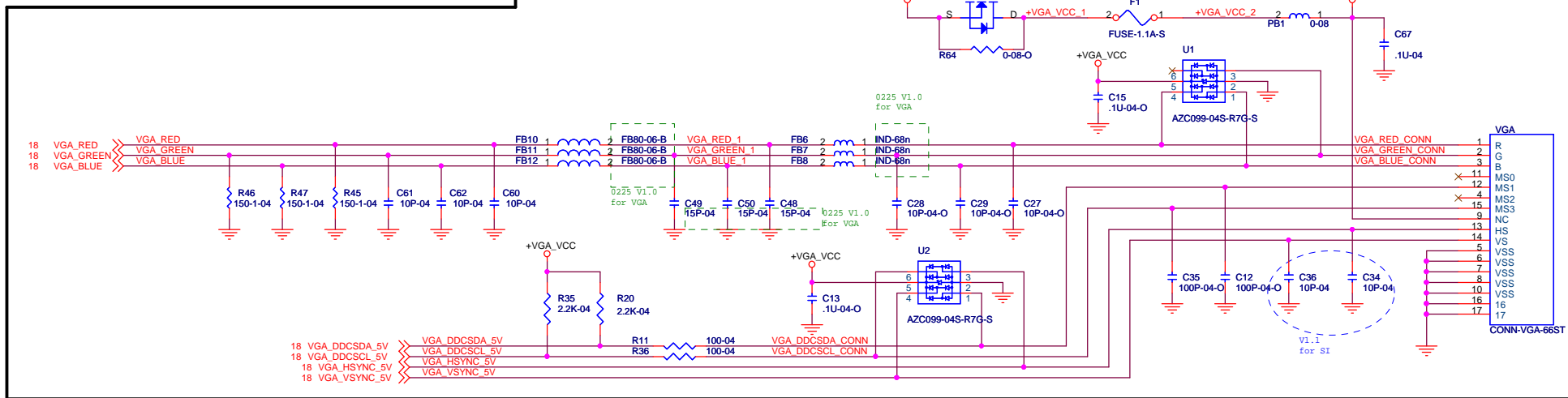
DESIGN NOTE:
DEFENSIVE DESIGN

PCH PIN	ES1	ES2	Production Systems
TDO	No Stuff	100 Ohms	51 Ohms
TMS	100 Ohms	100 Ohms	51 Ohms
TDI	100 Ohms	100 Ohms	51 Ohms
TRST#	10K Ohms	10K Ohms	51 Ohms
RJ24	0(2-3)	0(2-3)	0(1-2)

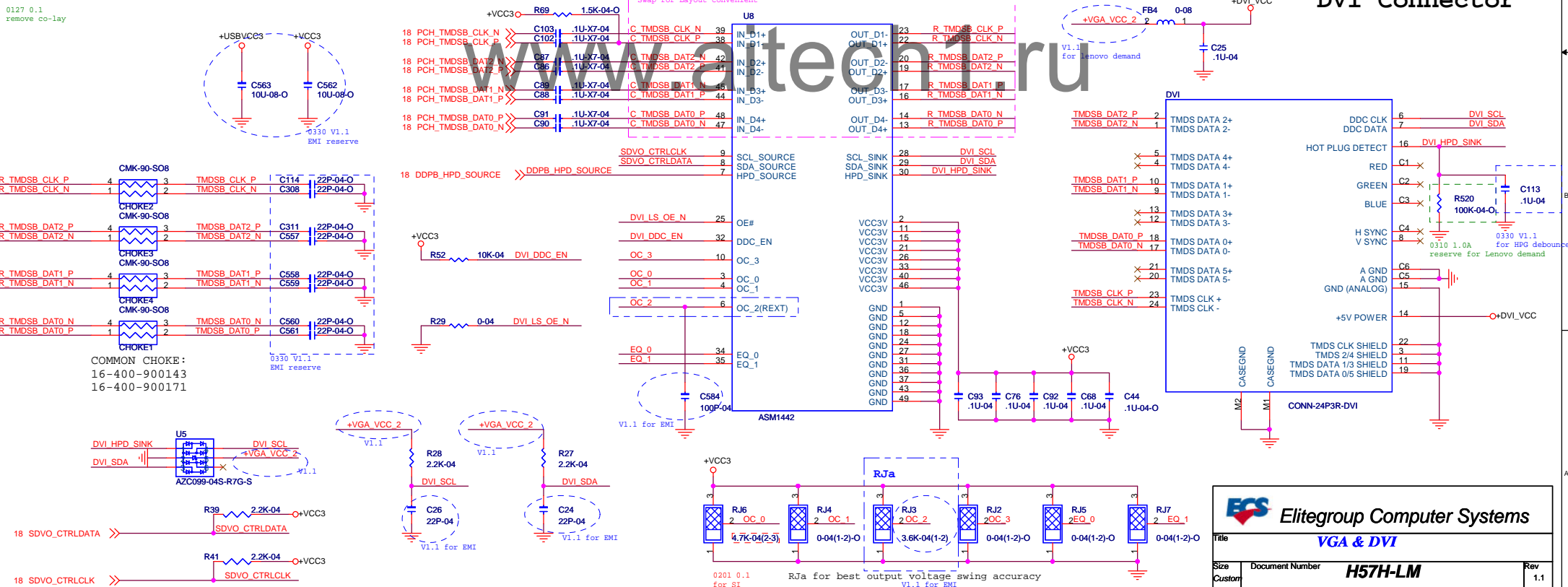
For Ix86-64 Platform --- non-inverting
 Asmedia : 02-342-442070 IC SWITCH.ASM1442..QFN48P.LEAD-FREE(RoHS) .ASMT
 NXP : 02-342-360121 IC SWITCH.FTN3360ABS..HVQFN48P.LEAD-FREE.NXP

For Eagle-Lake Platform--- inverting
 Asmedia : 02-342-442071 IC SWITCH.ASM1442T..QFN 48P.LEAD-FREE(RoHS) .ASMT
 NXP : 02-342-360120 IC SWITCH.FTN3360ABS..HVQFN 48P.LEAD-FREE.NXP

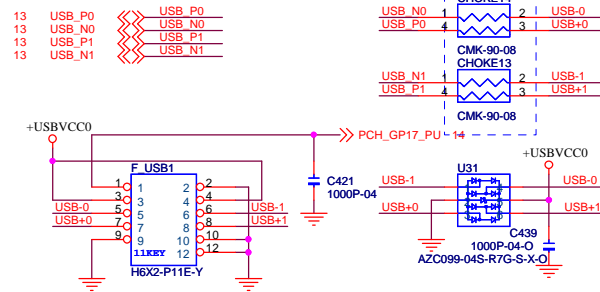
VGA Connector



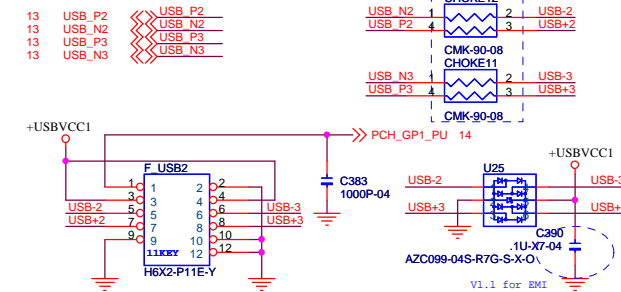
DVI Connector



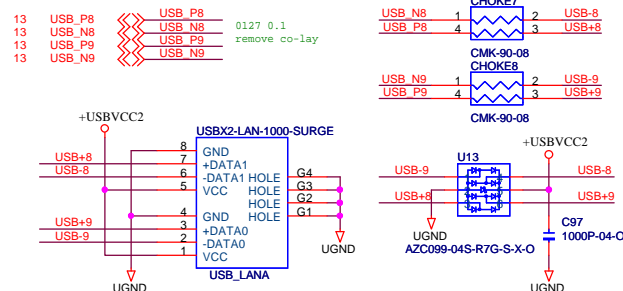
Front USB 1



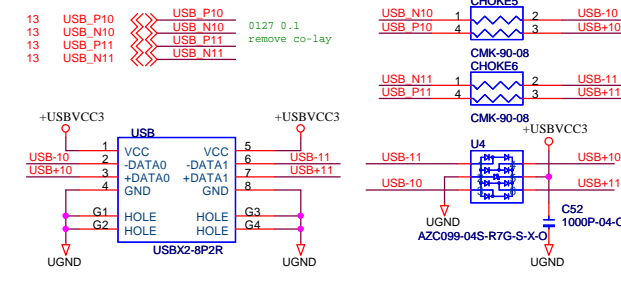
Front USB 2



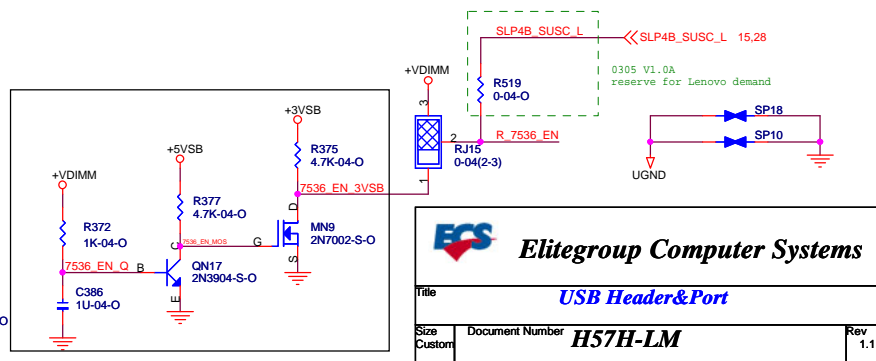
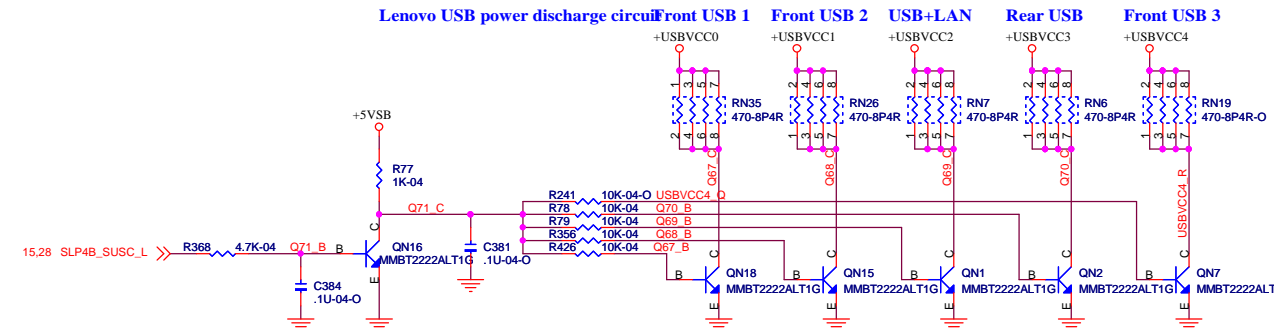
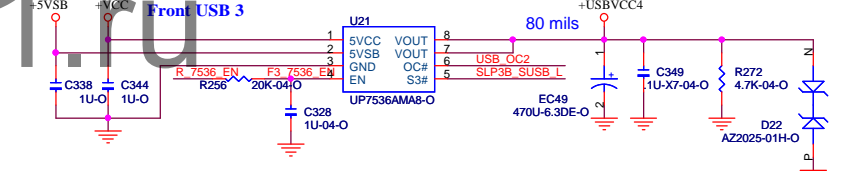
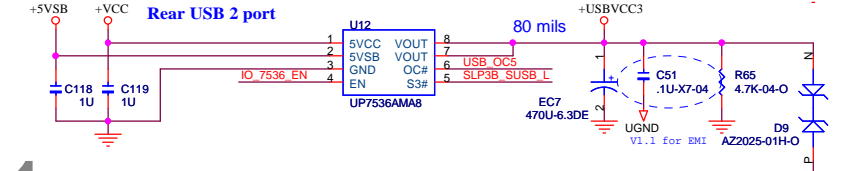
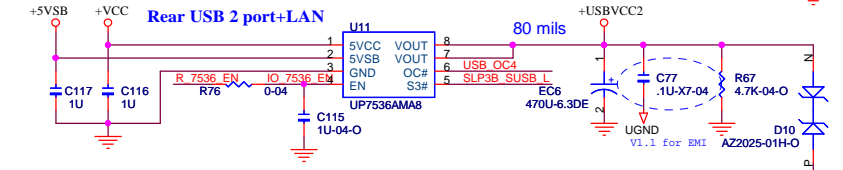
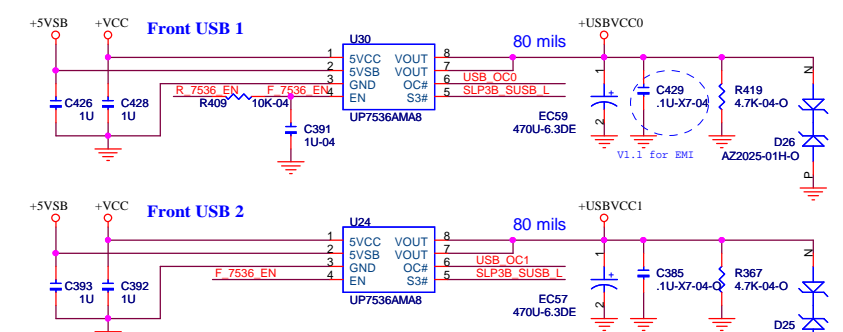
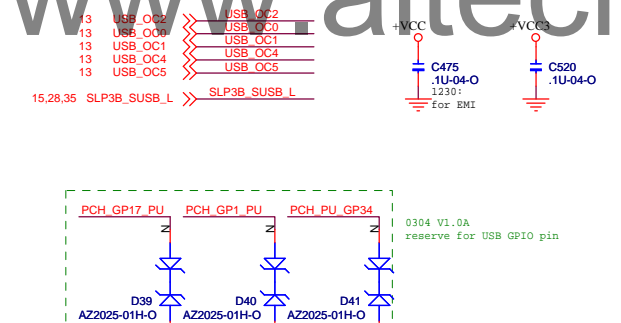
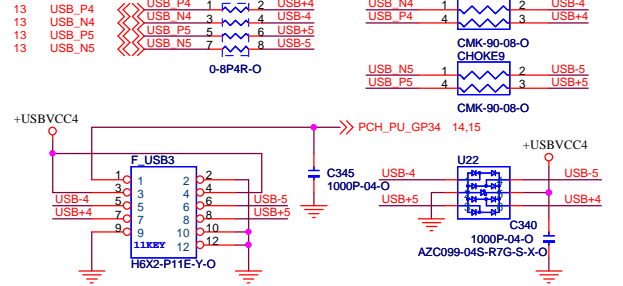
Rear USB 2 port+LAN



Rear USB 2 port



Front USB 3

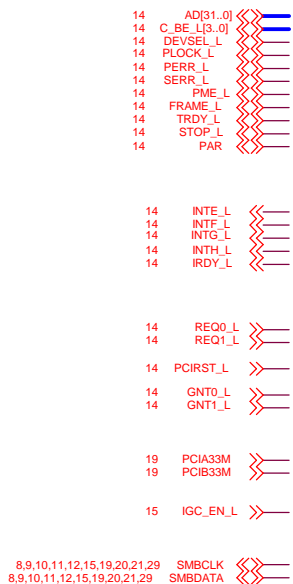


Elitegroup Computer Systems

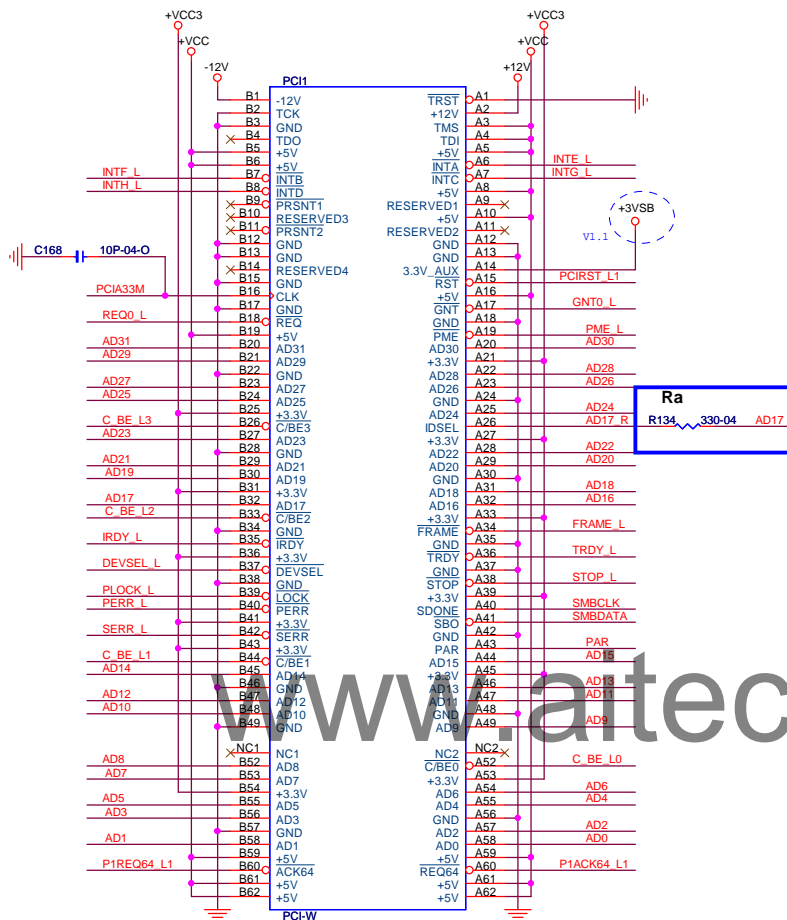
USB Header&Port

Size: Document Number **H57H-LM** Rev 1.1

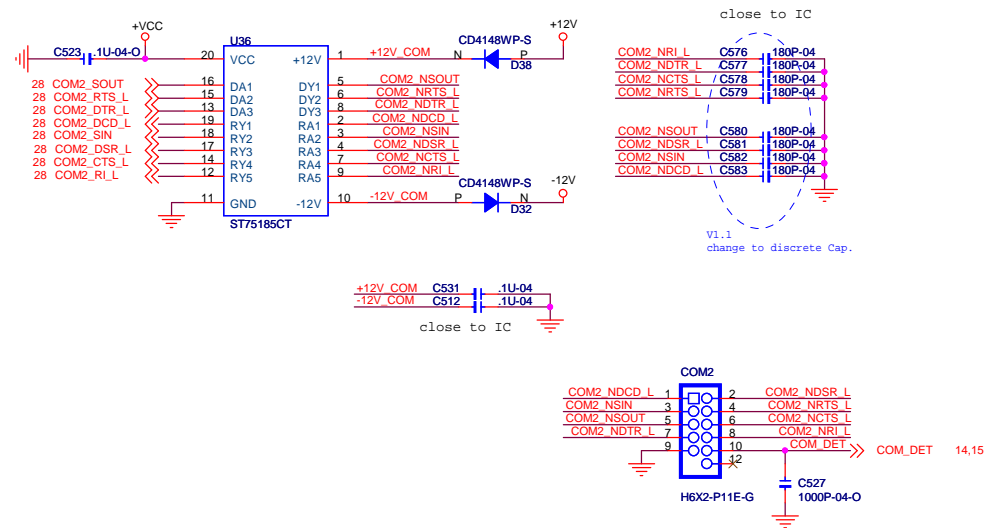
Date: Friday, April 02, 2010 Sheet 23 of 40



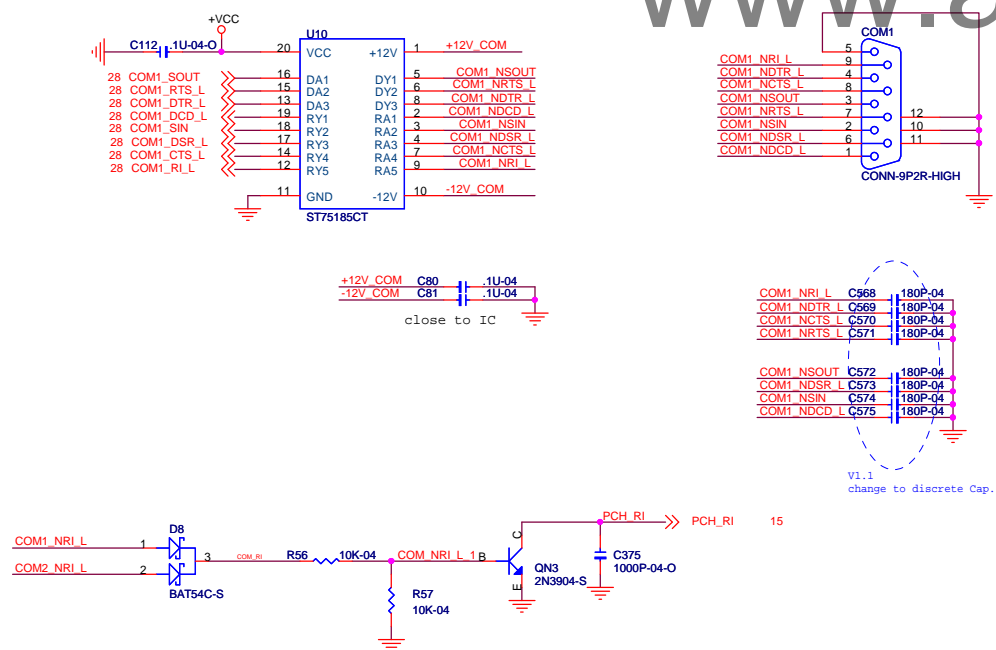
	PCI1	PCI2
INT	E	F
IDSEL	AD17	AD18
Ra	330-04	



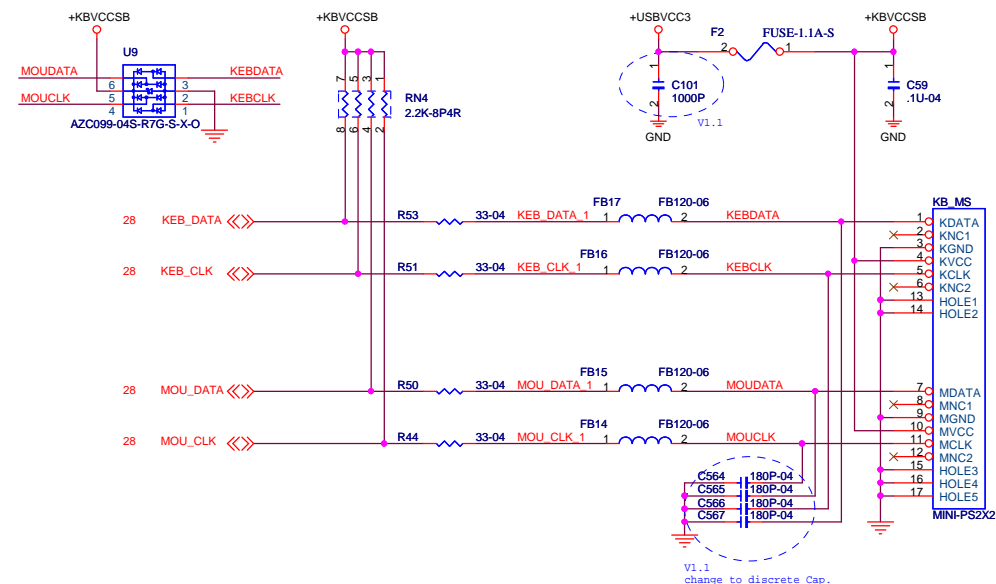
COM2



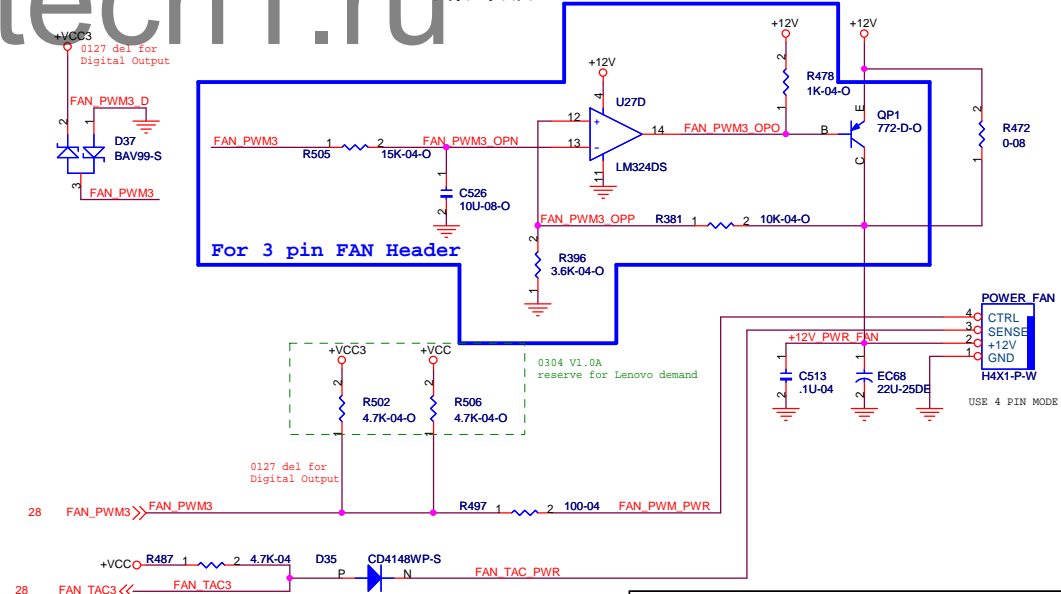
COM1



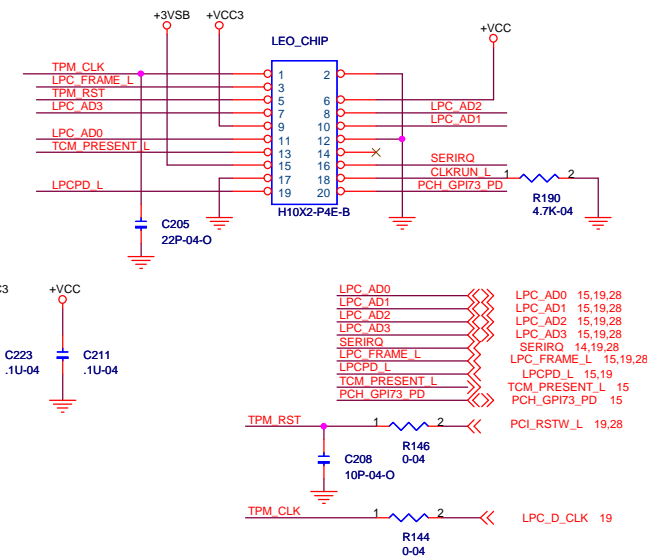
KEYBOARD & MOUSE



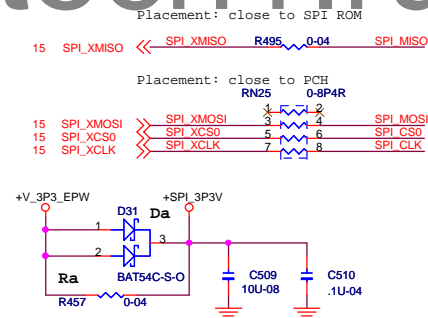
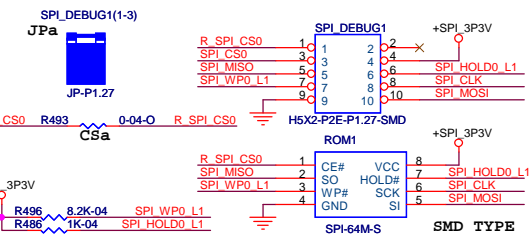
PWR FAN



TPM(or TCM) Header



SPI ROM



```
0210 0.1
del SPI ROM2
```

	for Lenovo debug card	for ECS bios debug	ET SDV	SIT
spi_debug1(2)	Stuff	Stuff	Stuff	n/c
JPa(b)	Stuff	n/c	Stuff	n/c
CSa(b)	n/c	Stuff	n/c	Stuff
Da	Da or Ra	Stuff	n/c	n/c
Ra	Da or Ra	n/c	Stuff	Stuff

01D530-064080

01D530-064110

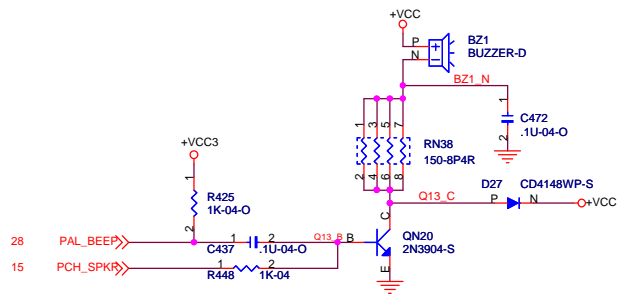


Size	Document Number	H57H-LM
Custom		

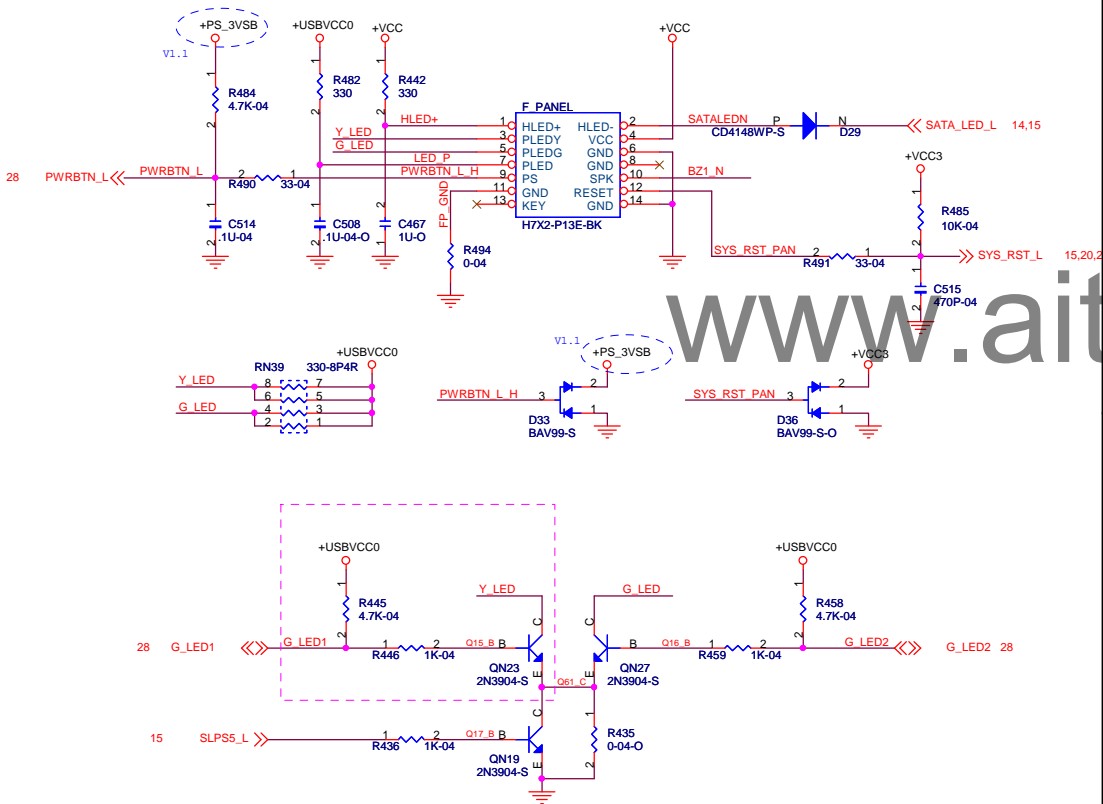
Date: Wednesday, April 07, 2010 Sheet 26 of 40

Rev	1.1
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BUZZER

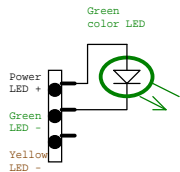


Front PANEL



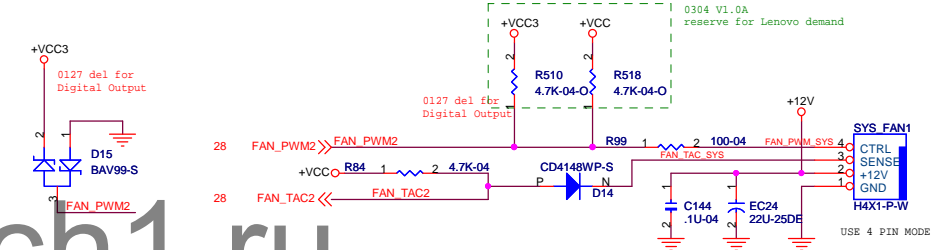
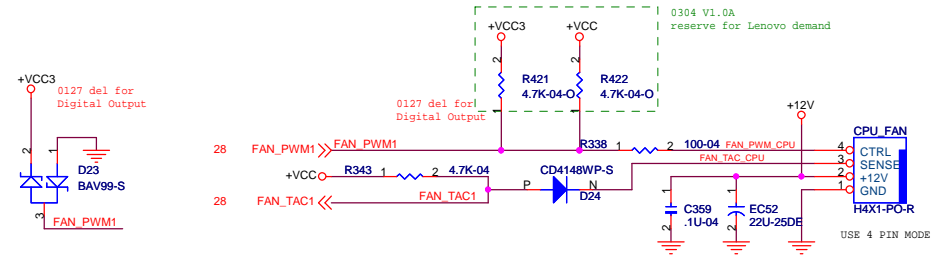
Lenovo LED

2-Pin single color LED	
S0	Steady Green
S1/S3	Green Blinking (Frequency: 1Hz)
S4/S5	OFF

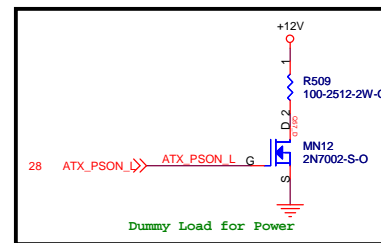
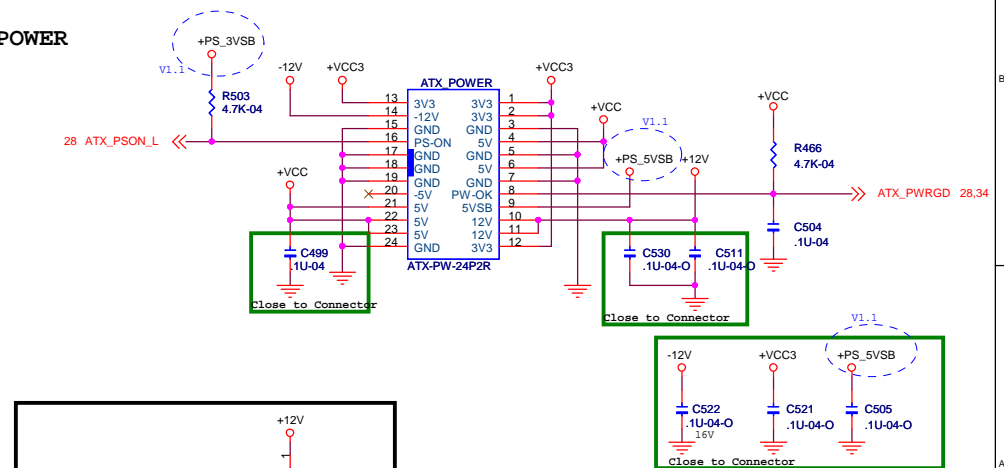


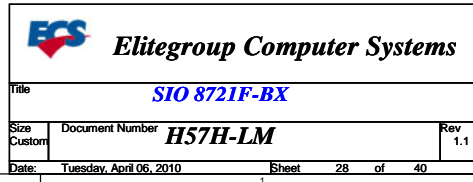
	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
Status	G	GB	YB	OFF	OFF
Remark	B:Blinking				

CPU/SYS Fan

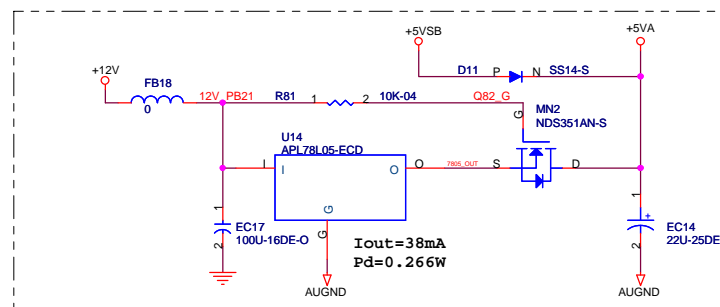


ATXPOWER

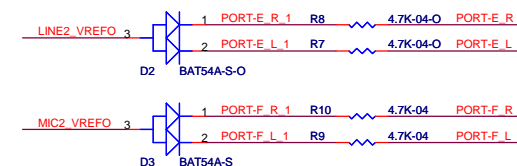




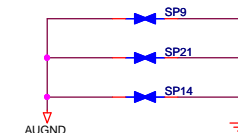
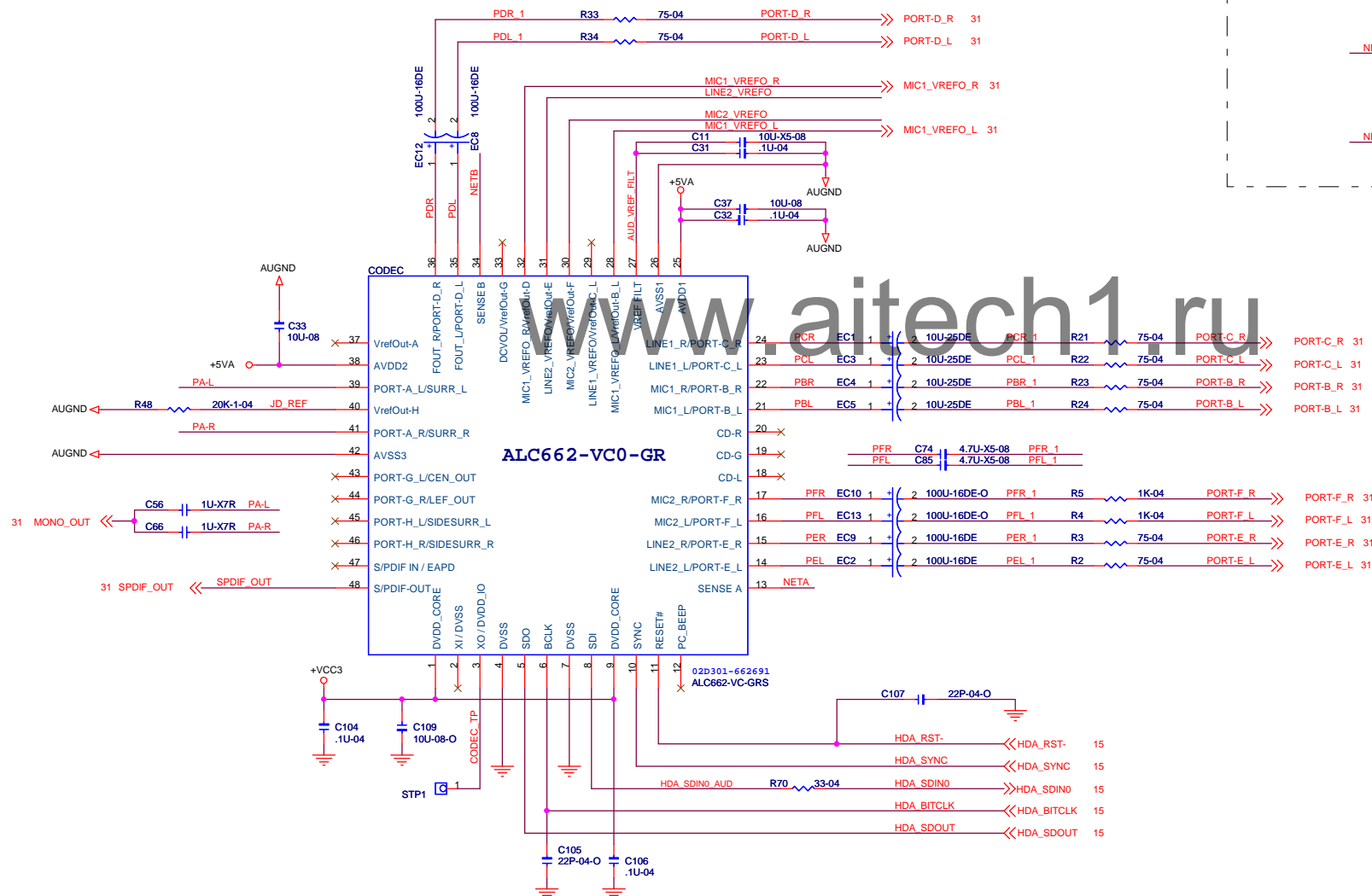
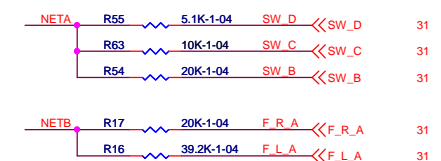

```
remove CODEC power control GPIO
```



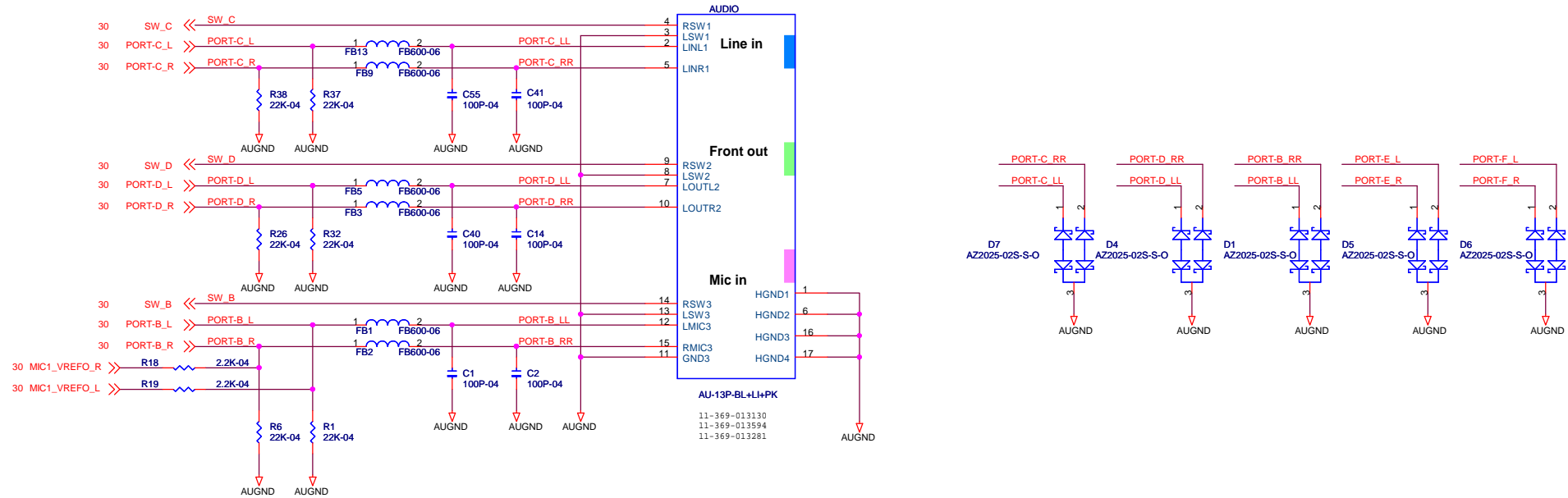
Place near Chip



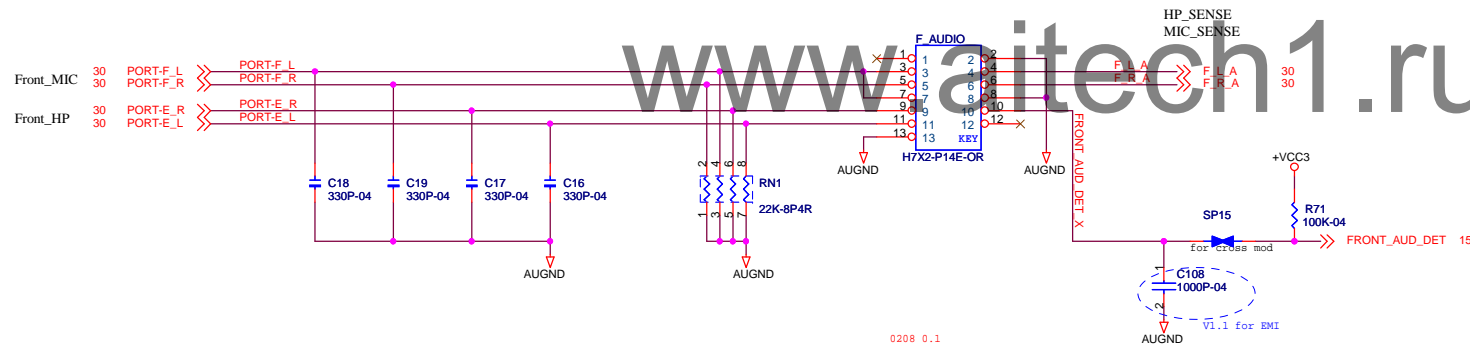
Place near Chip



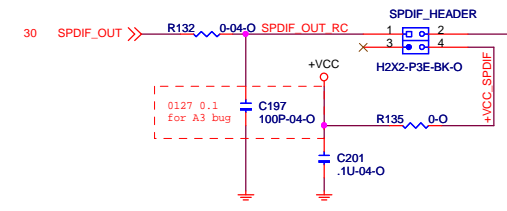
Rear AUDIO



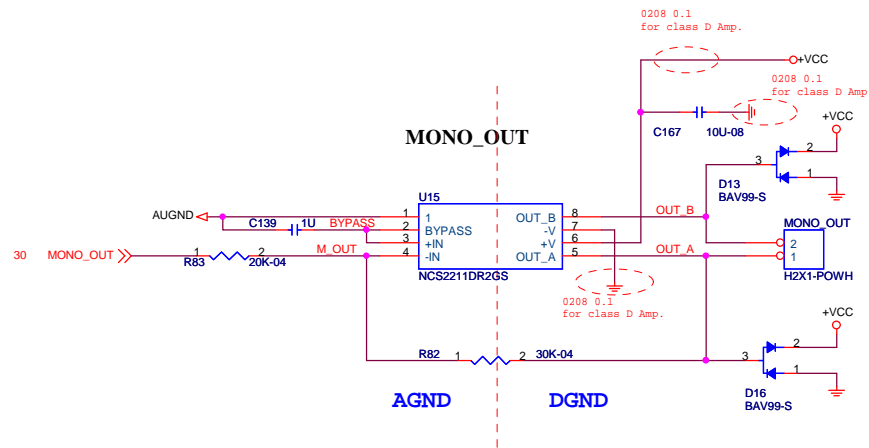
Front AUDIO

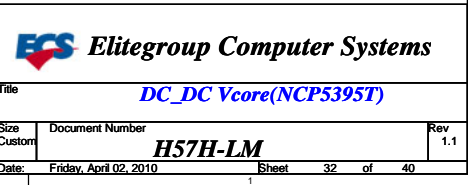


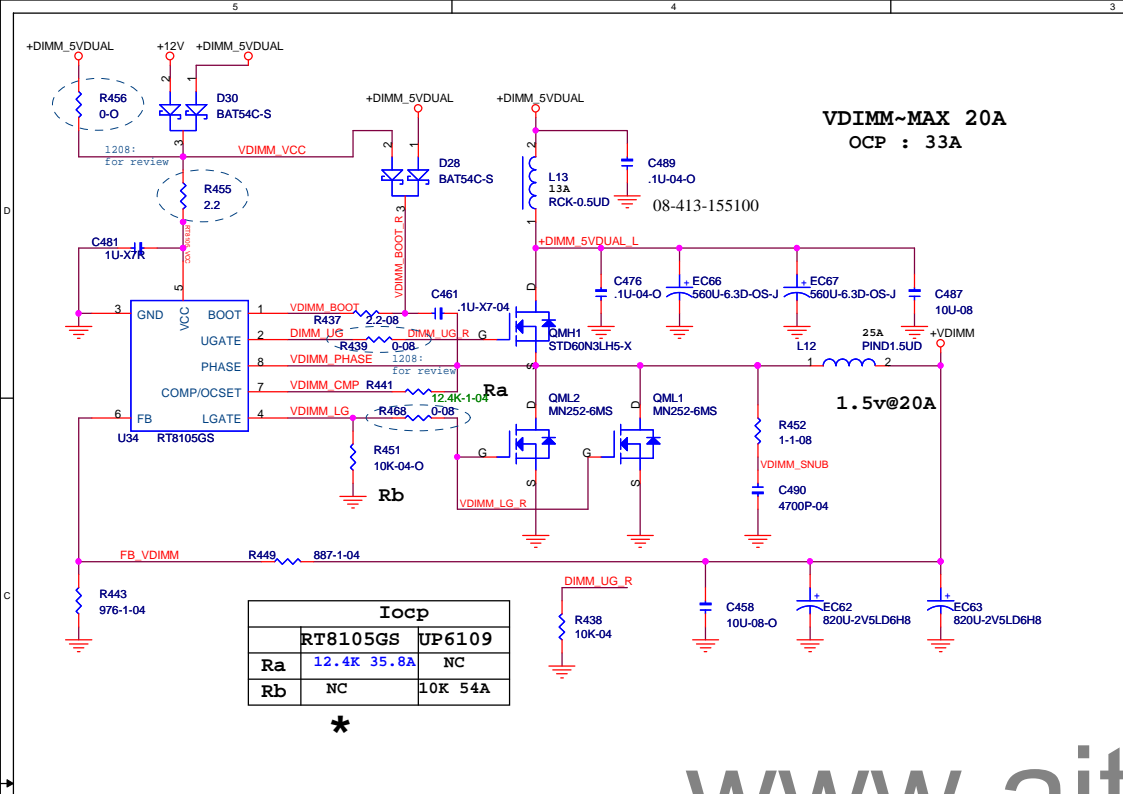
SPDIF OUT



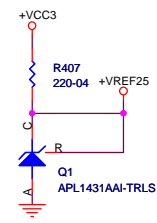
MONO_OUT



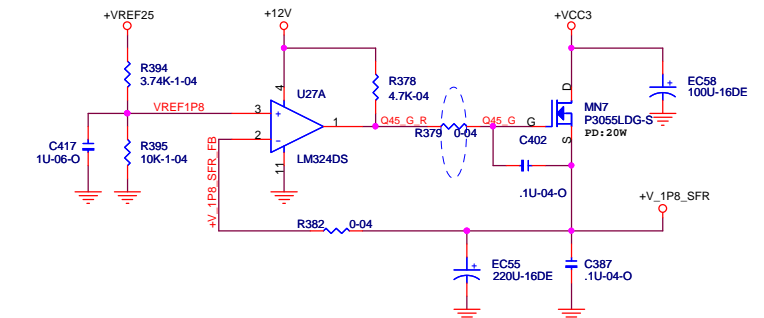




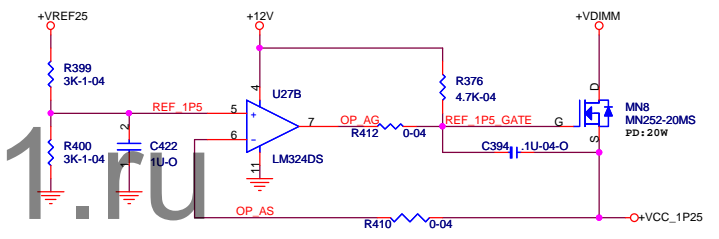
VREF25



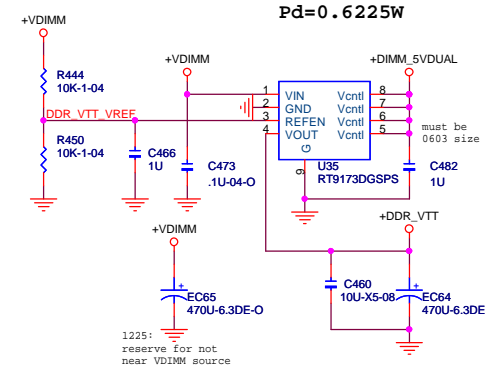
V_1P8_SFR 1.5A 2.25W



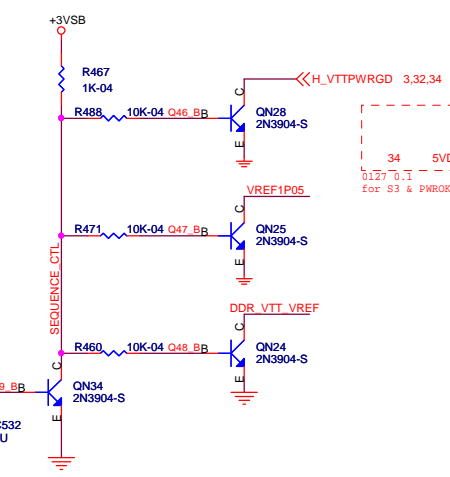
V_1P05_PCH Pd=1.625W



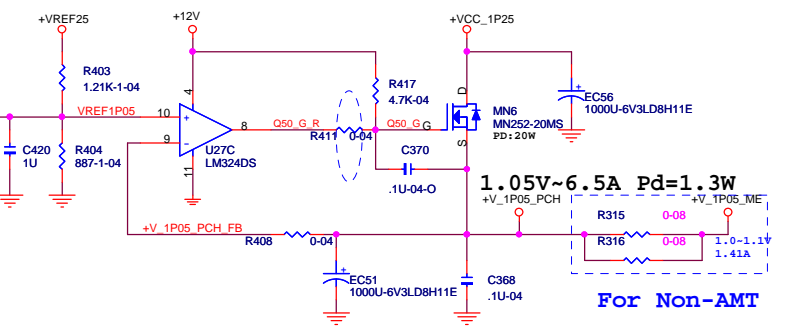
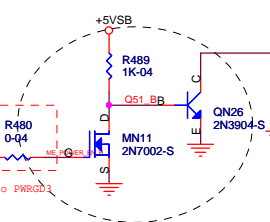
DDR_VTT DDR VTT~0.83A (DDR3) Pd=0.6225W



S3 shut down power circuit

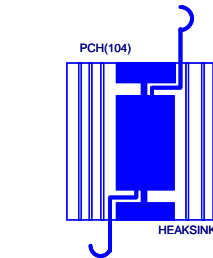


delay circuit

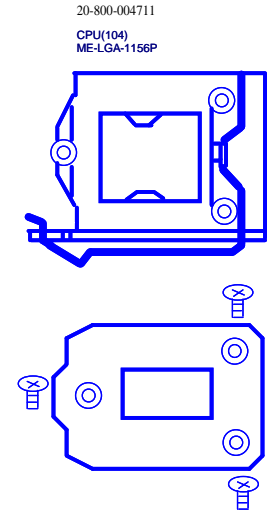


PCH

Name	Type	Voltage	Default	Functional Description	Function
GPIO22	I/O	+VCC3	Input	SCLOCK/GPIO22	CLR_CMOS_GP22
GPIO13	I/O	+3VSB	Input	GPIO13	LPC_PME_L
GPIO23	I/O	+VCC3	Native	LDRQ1#/GPIO23	FRONT_AUD_DET
GPIO32	I/O	+VCC3	Output	GPIO32	COM_DET
GPIO17	I/O	+VCC3	Input	TACH0/GPIO17	PCH_GP17_PU(F_USB1 DET)
GPIO1	I/O	+VCC3	Input	TACH1/GPIO1	PCH_GP1_PU(F_USB2 DET)
GPIO61	I/O	+3VSB	Output	SUS_STAT#/GPIO61	LPCPD_L(TPM or TCM LPCPD pin)
GPIO44	I/O	+3VSB	Native	PCIECLKRQ5#/GPIO44	TCM_PRESENT_L(Leo chip DET)
GPIO72	I/O	+3VSB	Native	PCIECLKRQ0#/GPIO73	PCH_GP173_PD(Leo chip GPIO)
GPIO38	I/O	+VCC3	Input	SLOAD/GPIO38	PCH_GP38_PU(LPT DET)
GPIO34	I/O	+VCC3	Input	STP_PCI#/GPIO34	PCH_PU_GP34(F_USB3 DET)
GPIO11	I/O	+3VSB	Native	SMBALERT#/GPIO11	PCH_PORT80_LED(PC12 wake up)
GPIO12	I/O	+3VSB	Native	LAN_PHY_PWR_CTRL/GPIO12	TP_GPIO_12(PCIE-1X wake up)

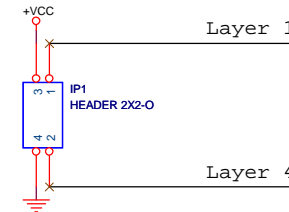


Main:add new P/N



ITE8721

Name	Type	Voltage	Functional Description	Function
GP34	I/O	+VCC3	GP34	GPIO_CASE0
GP35	I/O	+VCC3	GP35	GPIO_CASE1
GP23	I/O	+3VSB	GP23/SI	G_LED1
GP22	I/O	+3VSB	GP22/SCK	G_LED2
3VSBSW	I/O	+3VSB	3VSBSW#/GP40	GPIO40_S4S5
GP63	I/O	+VCC3	VCORE_GOOD/GP63	4/2 DIMM select
GP64	I/O	+VCC3	VCORE_EN/GP64	BS3 (reserve default PU)
GP65	I/O	+VCC3	VDDA_EN/GP65	BS1 (reserve default PU)
GP66	I/O	+VCC3	VLDI_EN/GP66	BS2 (reserve default PU)
GP67	I/O	+VCC3	CPU_PG/GP67	BS4 (reserve default PU)



1080 : trace width 4 mil 50 ohm
Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W

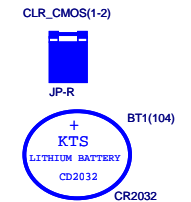
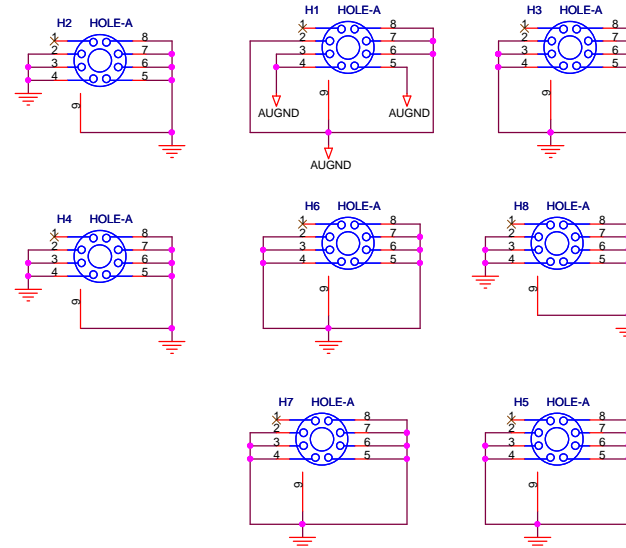
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Table 8-3. Measured I_{CC} (Desktop Only)

Voltage Rail	Voltage (V)	S0 Iccmax Current Integrated Graphics (A)	S0 Iccmax Current External Graphics (A)	S0 Idle Current Integrated Graphics (A)	S0 Idle Current External Graphics (A)	Sx Iccmax Current (A)	Sx Idle Current (A)	G3
V_CPU_IO	1.1/1.05	.001	.001	.001	.001	—	—	—
V5REF	5	.001	.001	.001	.001	—	—	—
V5REF_Sus	5	.001	.001	.001	.001	.001	—	—
Vcc3_3	3.3	.305	.305	.035	.035	—	—	—
VccADAC	3.3	.075	.0011	.0011	.0011	—	—	—
VccADPLLA	1.05	.1100	.0440	.1034	.022	—	—	—
VccADPLLB	1.05	.1100	.0440	.022	.022	—	—	—
VccCore	1.05	1.76	1.584	.528	.44	—	—	—
VccDMI	1.1	.063	.063	.0011	.0011	—	—	—
VccIO	1.05	3.482	2.862	.9504	.519	—	—	—
VccLAN	1.05	.253	.253	.091	.091	.165	—	—
VccME	1.05	1.41	1.41	.493	.493	1.22	.0044	—
VccME3_3	3.3	.0308	.0308	.0022	.0022	.0154	.0022	—
VccpNAND	1.8	.0055	.0055	.0022	.0022	0	0	—
VccRTC	3.3	.0011	.0011	.0011	.0011	.0011	.0011	6 uA See notes 1, 2
VccSus3_3	3.3	.0924	.0924	.0154	.0154	.1551	.0330	—
VccSusHDA	3.3	.0088	.0088	.001	.001	.001	.001	—
VccVRM	1.8/1.5	.169	.123	.129	.052	—	—	—

NOTES:

- G3 state shown to provide an estimate of battery life.
- I_{CC} (RTC) data is taken with VccRTC at 3.0 V while the system in a mechanical off (G3) state at room temperature.



Elitegroup Computer Systems		
GPIO Table & Other		
Title Size Custom	Document Number H57H-LM	Rev 1.1
Date: Friday, April 02, 2010		
Sheet 36 of 40		

ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

ATX4P1
12V
+/-5%

PIMOS
+NMOS

CONTROL

S0 State														
Device	Device On	EP	DSP	End Point Volt	DSP Volt	FSP	Max load/camp	Low	TM	Env	P_out (Watt)	L_in		
MB Configuration Parts (MB Level)														
Table.1 Original Power Source Consumption														
ATX-Source1	N/A	3V		9	11.9		11.94	100%			97.0			
ATX-Source2	N/A	VCC3G3		3.3			11.94	100%			38.41			
ATX-Source3	N/A	12V (2x1)	N/A	12			6.33	100%	N/A	N/A	75.86			
ATX-Source4	N/A	12V (2x2)		12			6.17	100%			88.84			
ATX-Source5	N/A	-12V		12			6.87	100%			8.84			
ATX-Source5	N/A	5VSB		5			1.43	100%			7.19			
TOTAL vWATT											387.0			

X1 PCIe per	X16 PCIe per
3.3V 3.0A	3.3V 3.0A
12V 0.5A	12V 5.5A
3.3Vaux 0.375A	3.3Vaux 0.375A

X16 PCIe per	PCI slot per
3.3V 3.0A	3.3V 7.6A
12V 5.5A	5V 5.0A
3.3Vaux 0.375A	12V 0.5A
	3.3Vaux 0.375A
	-12V 0.1A

USB X6 FR	USB X4 IO	2XPS/2
VDD 2.0A	VDD 2.0A	5VDual 1.0A
5VDual 2.0A	5VDual 2.0A	

AUDIO ALC662-VC0		
DVDD 3.3V	3.3V	40mA
AVDD	5V	51mA

Realtek LAN 8111E		
VDD3	3.3V	0.07A
+VDDIO	1.05V	0.3A

CLOCK ICS9LRS4180		
+VCC3	3.3V	120mA

SUPER I/O IT8721F-DX		
3VSB	3.3V	6mA
VCC3	3.3V	10mA
BAT 3.3V	3.3V	2uA

Intel Havendale/Lynnfield CPU		
VCCP	V1D 0.65~1.4V	90A(95W)
VAXG	V1D 0.8~1.3V	16A
VTT	1.1V	30A
VDDQ	1.5V	20A
VCCPLL	1.8V	1.35A
Vsm_Vtt	0.75V	1A

Intel Ibox Peak (TDP 6W)		
VccCore	1.05V	1.629A
VccIO	1.05V	3.251A
VccDMI	1.1V	0.065A
VccAPLLEXP	1.05V	VccVRM
VccSATAPLL	1.05V	VccVRM
VccADPLLA	1.05V	0.075A
VccADPLLB	1.05V	0.075A
VccVRM	1.8V	0.196A
VCCPNAND	1.8V	0.156A
_V5REF	5V	<1 mA
_V5REF_SUS	5V	<1 mA
VCCSUS3_3	3.3V	0.168A
VccSusHDA	3.3V	0.006A
V_CPU_IO	1.1V	< 1 mA
VccME3.3	3.3V	0.086A
VCC_ME	1.05V	2.222A
VccLAN	1.05V	0.372A
Vcc3_3	3.3V	0.357A
VCCRTC	3.3V	2 mA
VccADAC	3.3V	0.069A
VccFDIPLL	1.1V	VccVRM
VccACIK	1.1V	VccVRM

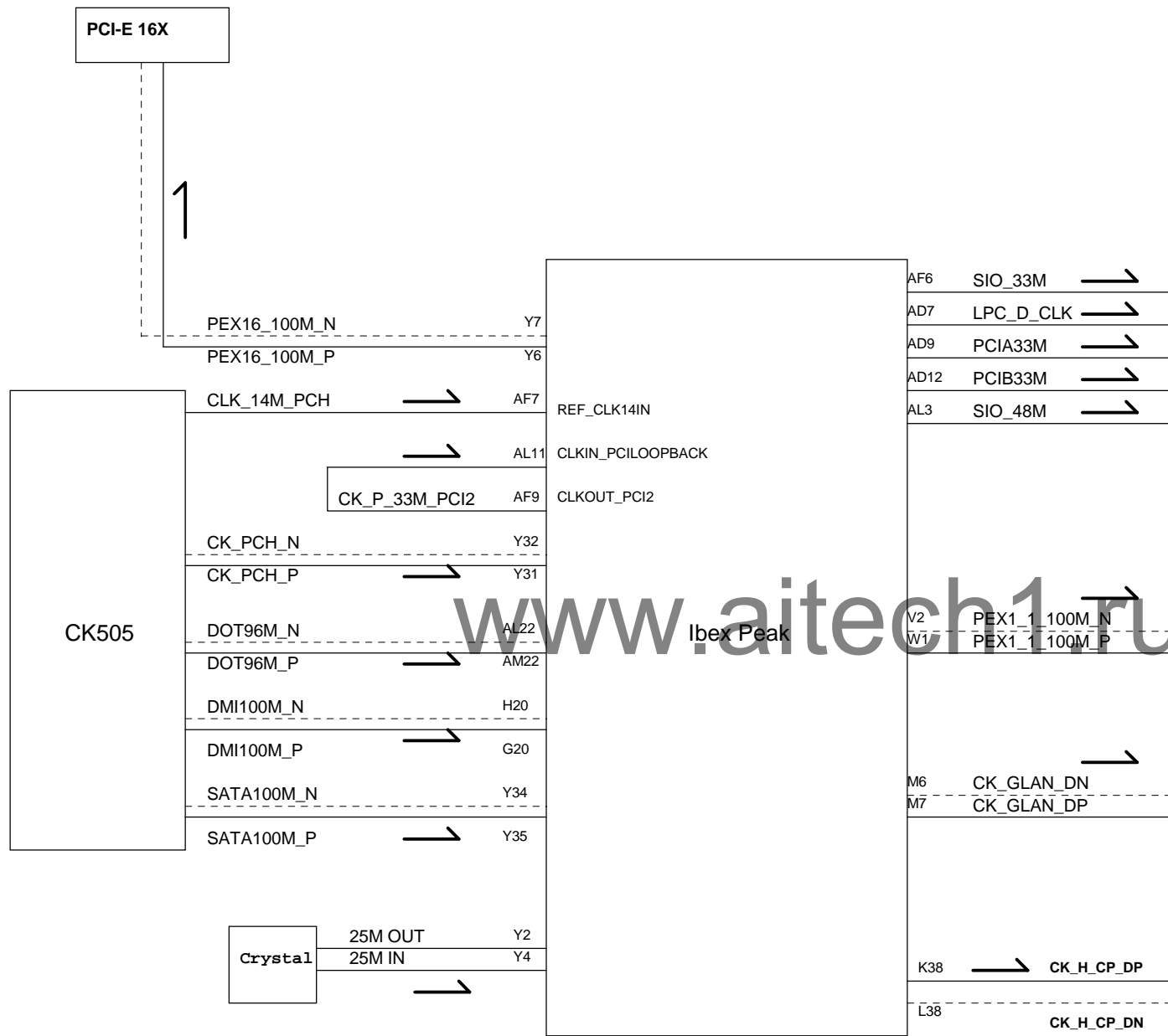
VCCRTC 3.3V

BATTERY




Elitegroup Computer Systems

Title	Power Delivery	
Size	Document Number	H57H-LM
Customer		Rev 1.1
Date:	Friday, April 02, 2010	Sheet 37 of 40



CHANGE HISTORY:

Rev	Date	Notes	Rev	Date	Notes
V0.1	2010/01/27	P23 remove RN5/RN8 co-lay ,P22 remove RN2/RN3 co-lay P32 C161 move to C123,BOM Vcore/VTTC/DIMM ST change to IR for power recommend P32 R150-->18.7K,R149-->10.5K for power recommend P31 C197 open for A3 SPDIF function test P28 U32 change to 8721F-DX,PWROK change to PWRGD3 for S3 fail, ATXPG level shift reserve +3VSB PU & add C534 P35 del R479,mount R480 for S3 fail P29 L1 change footprint	DCN_0999	2010/03/19	P29 reserve SMC2.0 (reserve EEP1)
	2010/02/01	P22 L1 RJ3(1-2) 3K,RJ6(2-3) 4.7K for SI P34 mount R481 for ACPI power measurement,U33 change to 1085 for Eup P28 QN22 change to MN13 can unmount C534	DCN_1004	2010/03/19	P19 R243 change to 47 ohm for SI SIO_48M P15 C366,C367 change to 15pF for RTC
	2010/02/06	P24 PCI2 wake up event change to GPIO11 for BIOS Spec. P8 PCIE-1X wake up event change to GPIO12 for BIOS Spec. P28 add QN35 C536 for Spec. update			
	2010/02/09	P26 add CI-1			
V1.0	2010/02/11	From V0.1 change to V1.0 P30 reserve GPIO control standby power P29 swap LAN LED connector pin for Lenovo Spec.			
	2010/02/25	P22 FB10,FB11,FB12 change to FB80,FB6,FB7,FB8 change to IND-68n,C48,C49,C50 change to 15pF for VGA signal P33 add C121,C127 for VGA noise P34 add C147,C189 for VGA noise			
V1.0A	2010/03/04	P15 reserve C361 for lenovo demand P23 reserve D39,D40,D41 for USB GPIO pin P25 reserve R502,R506 for Lenovo demand P27 reserve R421,R422,R510,R518 for Lenovo demand P19 Asset ID from VCC3 change to 3VSB for Lenovo demand P9,10,11,12 change DIMM silkscreen from DIMM1,2,3,4 to DIMM2,1,4,3			
	2010/03/05	P23 reserve R519 for Lenovo demand			
	2010/03/10	P22 reserve R520 for Lenovo demand			
	2010/03/11	P26 LPT header change footprint			
V1.1	2010/03/24	P8, P15,P24,P27,P28,P29,P30,P34 reserve Eup function : +PS_5VSB & +PS_3VSB switch circuit			
	2010/03/29	P26 CN6,CN7,CN8,CN9 change to discrete Cap.			
	2010/03/30	P22 Dvi_Hpd_Sink & signal reserve Cap. to GND for EMI +VCC3 & +USBVCC3 reserve Cap. for EMI			
	2010/04/01	P22 RJ3 change to 3.6K,C24,C26 22pF for EMI P23 C51,C77,C390,C429 0.1uF,remove RN31,RN36, add choke11,choke12,choke13,choke14 for EMI P31 C108 1000pF for EMI P25 CN1,CN2,CN3,CN4,CN5 change to discrete Cap. P22 add C584 for EMI P29,P24,P15 change LAN SMLink0 to SMBUS, SM0ALERT to SMALERT,PCI2 GPIO change to GPIO8 P22 FB4 change connect to +VGA_VCC_2			
	2010/04/02	P25 C101 1000PF for EMI P22 C34,C36 10pF for SI P29 reserve SMLINK1/DAT/ALERT to LAN SMBUS/ALERT P28 C434 100pF for SI			

		Elitegroup Computer Systems	
Title		<i>History</i>	
Size	Document Number	Rev	
Custom	H57H-LM	1.1	
Date:	Wednesday, April 07, 2010	Sheet	40 of 40